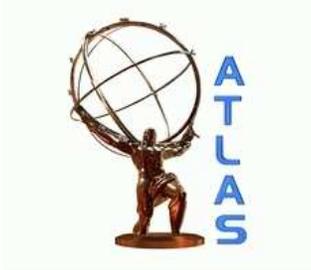


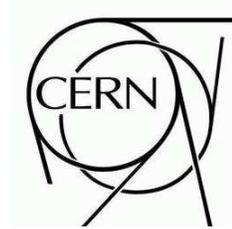
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ATLAS NOTE

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December 20, 2007



The ATLAS Pixel Detector

The Pixel Collaboration

Abstract

1 Introduction

This paper describes the pixel detector system for the ATLAS experiment at the Large Hadron Collider (LHC). The ATLAS detector is a general purpose detector for the study of primarily proton-proton collisions at the LHC [?]. The pixel detector system is a critical component of the inner tracking detector of ATLAS [?]. The ATLAS Inner Detector (ID) provides highly efficient charged-particle track reconstruction over the pseudorapidity range $|\eta| < 2.5$ [87]. The pixel detector, with approximately 80 million channels, is essential to provide pattern recognition capability to meet the track reconstruction requirements of ATLAS at the full luminosity of the LHC of $\mathcal{L} = 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. The pixel detector system is the innermost element of the Inner Detector. It is therefore the most important contributor to the precision needed for efficient identification and reconstruction of secondary vertices from the decay of, for example, particles containing a b-quark and for b-tagging of jets. In addition, it provides the excellent spatial resolution necessary for reconstructing primary vertices in the proton-proton interaction region within ATLAS even in the presence of the many multiple interactions present at the LHC design luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$.

In the sections below, we first present the performance requirements for the pixel detector. This is followed by an overview of the system and its relationship to the Inner Detector. We then describe in detail the principal components of the pixel detector system—electronics, sensors, modules, mechanical systems and services. Finally, we summarize results from test beam studies of the pixel components and the operation of about 10% of the pixel system using cosmic ray tracks.

2 Performance Requirements and Design Choices

The performance requirements of the ATLAS Inner Detector (ID) were formulated in the Inner Detector Technical Design Report (TDR) [?]. The pixel system is an important part of the ID and plays a major role in fulfilling these requirements.

The general performance requirements for the pixel system are:

- coverage of the pseudorapidity range $|\eta| < 2.5$;
- excellent transverse impact parameter resolution;
- good resolution on the longitudinal z -coordinate, allowing primary vertex reconstruction with charged tracks with $\sigma(z) < 1 \text{ mm}$;
- good 3D-vertexing capabilities;
- very good jet b-tagging capabilities both in the high level trigger and in the offline reconstruction;
- minimal material in all elements of the system in order to reduce multiple scattering and secondary interactions;
- excellent efficiency of all pixel layers; and
- radiation hardness of the pixel detectors to operate after a total dose of 500 kGy or $10^{15} n_{eq}/\text{cm}^2$.

These performance requirements lead to the following major design choices:

- three pixel hits over the full rapidity range. The requirement to have three pixel layers has been confirmed by a detailed study comparing a layout with two pixel hits versus a layout with three pixel hits [?];

- minimal radius of the innermost layer (b-layer), set at 5 cm due to the practical limitations of clearances around the interaction region beam pipe vacuum system;
- the smallest pixel size, which was finally set to $50 \mu\text{m} \times 400 \mu\text{m}$ by electronics design limitations;
- the expected dose rate for the innermost layer is expected to reach 500 kGy after about the first five years of LHC operation. The other layers are expected to reach the 500 kGy dose after 10 or more years of LHC operation (with maximum luminosity of $10^{34} \text{cm}^{-2}\text{s}^{-1}$).

3 System Overview

In this section we present a brief overview of the pixel system and its relationship to the Inner Detector. The basic parameters of the pixel system are also summarized in this section.

The pixel detector is the innermost element of the Inner Detector as shown in Figure 1. The pixel tracker is designed to provide at least three points on a charged track emanating from the center of the collision region in ATLAS. The pixel detector and the other elements of the Inner Detector cover a pseudorapidity range $|\eta| < 2.5$.

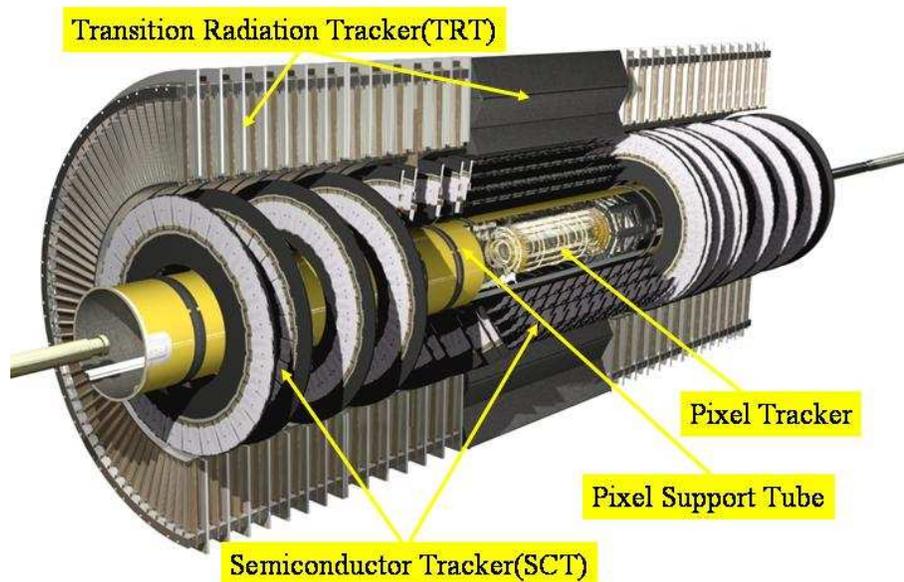


Figure 1: ****Placeholder*** Need different figure, more labels.

The principal components of the pixel tracking system are the following:

- active region of the pixel detector, which itself is composed of three barrel layers and a total of six disk layers, three at each end of the barrel region;
- internal services (power, monitoring and cooling) and their associated mechanical support structures (also supporting the interaction region beam pipe) on both ends of the active detector region;

- a Pixel Support Tube into which the active part of the pixel detector and the services and related support structures are inserted and located; and
- external services that are connected to the internal services at the end of the Pixel Support Tube.

The active region of the pixel detector is shown in a schematic view in Figure 2. The active part of the pixel system consists of three barrel layers—Layer 0 (so-called b-layer), Layer 1 and Layer 2—and two identical endcap regions, each with three disk layers.

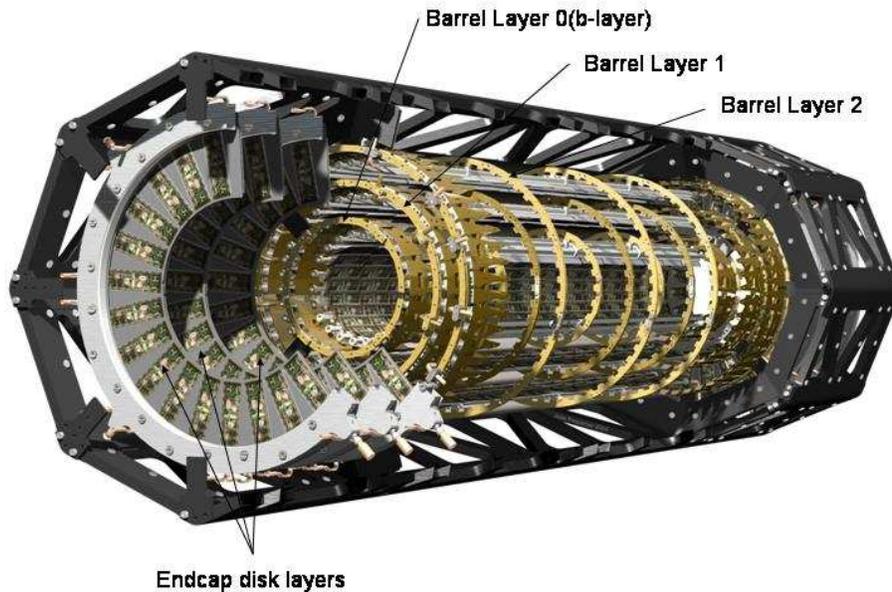


Figure 2: ***Placeholder*** Need higher res, better labels, already shown?

The basic building block of the active part of the pixel detector is a module (section ??) that is composed of silicon sensors (section ??), front-end electronics and μ ex hybrids with control circuits (section ??). All modules are functionally identical at the sensor/integrated circuit level but differ somewhat in the interconnection schemes for barrel modules and disk modules. The pixel size is 50 microns in the ϕ direction and 400 microns in z (barrel region, along the beam axis) or r (disk region) apart from a few special pixels in the overlap region between integrated circuits on a module—see sections ?? and ??. There are 46,080 pixels in each module.

The essential parameters of the barrel region of the pixel detector system are summarized in Table 1. Modules are mounted on mechanical/cooling supports, called staves, in the barrel region. Thirteen modules are mounted on a staff and the staff layout is identical for all layers. The active length of each barrel staff is about 801 mm. More details are given in section ??.

The two endcap regions are identical. Each is composed of three disk layers and each disk layer is identical. The basic parameters of the endcap region are given in Table 2. Modules are mounted on mechanical/cooling supports, called disk sectors. There are eight identical sectors in each disk.

The total number of pixels in the system is approximately 67 million in the barrel and 13 million in the endcaps, giving a total active area of about 1.7 m².

Layer Number	Mean Radius (mm)	Number of Staves	Number of Modules	Number of Pixels	Active Area (m ²)
0	50.5	22	286	13,178,880	0.28
1	88.5	38	494	22,763,520	0.49
2	122.5	52	676	31,150,080	0.67
TOTALS		112	1456	67,092,480	1.45

Table 1: Basic parameters of the barrel region of the ATLAS pixel detector system.

Disk Number	Mean z (mm)	Number of Sectors	Number of Modules	Number of Pixels	Active Area (m ²)
0	495	8	48	2,211,840	0.0475
1	580	8	48	2,211,840	0.0475
2	650	8	48	2,211,840	0.0475
TOTAL ONE ENDCAP		24	144	6,635,520	0.14
TOTAL BOTH ENDCAPS		48	288	13,271,040	0.28

Table 2: Basic parameters of the endcap region of the ATLAS pixel detector system.

The expected instantaneous fluence of charged hadrons in the Inner Detector volume is shown in Figure 3. One can see that the highest fluences are in the region of pixel detectors, requiring radiation hard sensors, radiation hard electronics and operation at low temperatures.

The contribution of the Pixel Detector to the total Inner Detector material budget as a function of pseudorapidity is shown in Figure 4 (radiation lengths) and Figure 5 (interaction lengths). The beam pipe contribution is also shown.

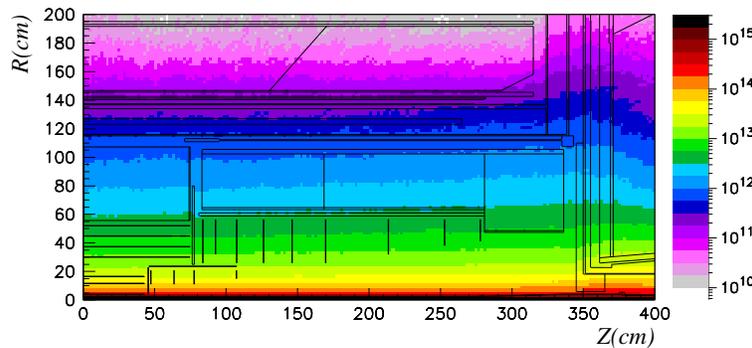


Figure 3: Fluence of the charged particles in the ID detector per cm² per year at the LHC design luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$. *** Placeholder ***

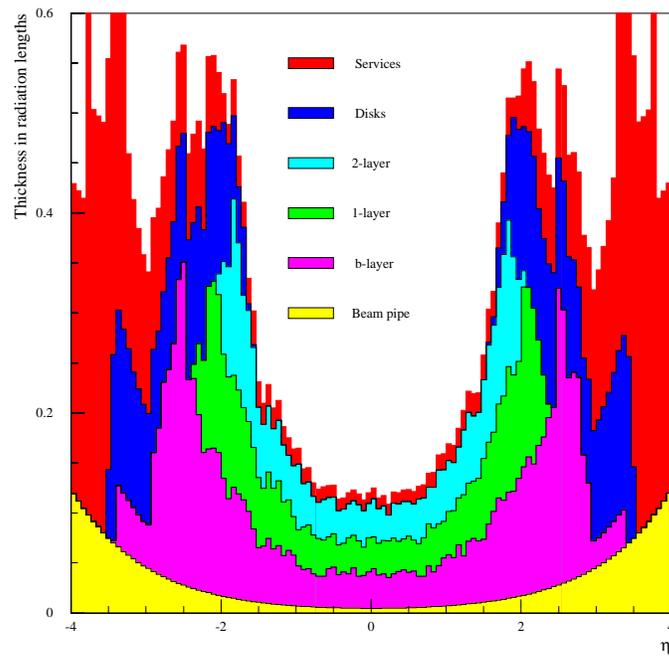


Figure 4: Material budget of the pixel detector in radiation lengths. *** Placeholder ***

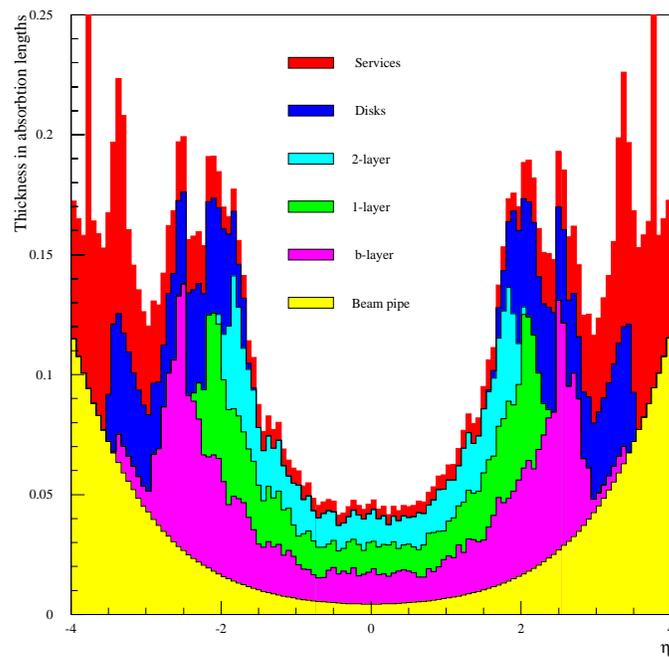


Figure 5: Material budget of the pixel detector in nuclear absorption lengths. *** Placeholder ***

4 Electronics Systems

4.1 Overview

The first comprehensive proposal of the pixel electronic system was described in 1997-98 in the ATLAS Inner Detector and Pixel Detector Technical Design Reports [1, 2]. The complete system underwent several revisions in the years to follow. The radiation tolerance required is 50 Mrad, corresponding to 10 years of operation at nominal LHC luminosity for the external layers and 3 years for the innermost layer (B-layer). The total number of instrumented channels is 80 million, each with about 1,000 transistors and 100 μW maximum power consumption (power for on-detector circuitry only).

4.1.1 System Architecture

A block diagram that illustrates the system architecture with the principal links to the blocks is shown in Fig. 6.

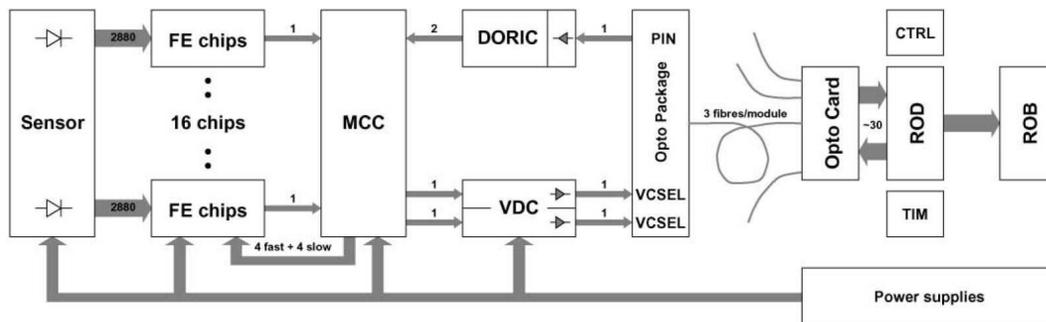


Figure 6: Simplified block diagram of the pixel detector System Architecture. (Original figure needed)

Charge released by ionizing particles in the cells of the sensor array are collected by 16 front-end chips (FE) per module, arranged in two rows of eight chips. The 16 FEs are read out by a Module Control Chip (MCC). Data are transmitted from FE to the MCC using Low Voltage Digital Signalling (LVDS) serial links, configured in a serial star topology. The serial protocol minimises the number lines to be routed, while the star topology maximizes bandwidth and reliability. Each module is then connected to the off-detector Read-out Drivers (ROD) through opto-links. One down link is used to transmit clock, trigger, commands and configuration data, while one or two up-links are used for event readout. The B-layer uses two up-links to increase the aggregate bandwidth needed for the higher average hit occupancy at the minimum radius. The readout (R/O) architecture is "data-push". This means that each component in the chain (FE, MCC) always transmits at the maximum rate and there is no busy mechanism to stop transmission when buffers are full. Each upstream component in the R/O chain (MCC, ROD) has always to monitor the number of events received and compare with the number of triggers sent. In case the difference of the two is bigger than a predefined value, triggers downstream are blocked and empty events are generated for the missing ones.

The power supply system uses commercial components, adapted to the requirements of the pixel detector, for the low (electronics) and high (sensor bias) voltages. The use of deep sub-micron electronics and long resistive cables with significant voltage drop, required the use of low voltage regulator boards near (10 m) the pixel detector; electronics can never see a voltage above maximum rating (4 V). To interface the electrical to the optical sides of the opto-links, special driver chips (DORIC and VDC) have been implemented and also an opto-card (Back of Crate or BOC) is used for each ROD.

4.2 Front-end Chip (FE)

4.2.1 Front-end Chip History

Small scale chips to demonstrate analog and digital architecture were developed in the second half of 1990s (M72b [3], Lepton [4], Marebo [5, 6] and Beer & Pastis [3, 7]). The first rad-soft functional prototypes of full size chips were submitted in 1998: FE-B at LBNL, FE-A/C (Pirate) at Bonn/CPPM. FE-B was designed using 0.8 μm HP CMOS technology and had the same basic readout architecture that is used in the final chips. The FE-B charge amplifier uses a direct cascode¹⁾ and source follower, feedback capacitance of 4 fF, DC feedback based on the Marebo design. The discriminator used a dual threshold, low threshold for precise timing and a high threshold to validate hit.

FE-A was made on 0.8 μm BiCMOS technology from AMS, whereas FE-C was a full CMOS version. The charge amplifier used a folded cascode input stage with feedback capacitance of 3 fF and a new improved DC feedback. The discriminator was AC coupled, with an input fully differential bipolar pair in the A version and CMOS in the C version. The column readout architecture used an always running shift register to transport the hit address to the bottom of the chip. Hits are associated to the level 1 trigger (L1) by counting the number of clock cycles needed for the hit to reach the column bottom. FE-A/B/C demonstrated all the basic ATLAS pixel performance goals in the laboratory and beam. The subsequent chip was developed using the basic concept of the amplifier/discriminator from FE-A/C and the column readout architecture from FE-C. The European and US front-end design efforts joined forces to combine all of the experience gained with radiation-soft chips into a common layout for the DMILL²⁾ "Durci Mixte sur Isolant Logico-Lineaire" technology (known as FE-D). FE-D1 was submitted in July '99 together with DORIC and VDC chips and a prototype MCC-D0. A new production run was submitted in Aug '00 with two versions of FE-D2: one with dynamic and the other with static memory cells. This run included the full MCC-D2 and new DORIC and VDC chips as well. Yields of both FE and MCC were unacceptable and work with this vendor was terminated. Work on FE-H began in Dec 1999 [8]. The chip was almost ready but was never submitted also because of massive cost increases from Honeywell. The failure of both traditional rad-hard vendors left the collaboration with the Deep Sub-micron (DSM) approach, based on commercial process 0.25 μm CMOS and rad-tolerant layout. A major design effort initiated in Sep 2000. Three versions (FE-I1, FE-I2 and FE-I3) were submitted using the 0.25 μm DSM process. The final chip (FE-I3) was available in late 2003. Table 3 gives a summary of the front-end designs developed for the ATLAS pixel detector.

Chip	Year	Cell size (μm^2)	Col \times Row	Transis- tors	Technology	References
Beer & Pastis	1996	50 \times 436	12 \times 63	–	AMS 0.8 μm BiCMOS, 2M	[3, 7]
M72b	1997	50 \times 536	12 \times 64	–	HP 0.8 μm CMOS, 2M	[3]
Marebo	1997	50 \times 397	12 \times 63	0.1 M	DMILL 0.8 μm BiCMOS, 2M	[5, 6]
FE-B	1998	50 \times 400	18 \times 160	0.8 M	HP 0.8 μm CMOS, 2M	[8–10]
FE-A/C	1998	50 \times 400	18 \times 160	0.8 M	AMS 0.8 μm BiCMOS, 2M	[7, 10]
FE-D1	1999	50 \times 400	18 \times 160	0.8 M	DMILL 0.8 μm BiCMOS, 2M	[10]
FE-D2	2000	50 \times 400	18 \times 160	0.8 M	DMILL 0.8 μm BiCMOS, 2M	–
FE-I1	2002	50 \times 400	18 \times 160	2.5 M	DSM 0.25 μm CMOS, 6M	[11]
FE-I2/I2.1	2003	50 \times 400	18 \times 160	3.5 M	DSM 0.25 μm CMOS, 6M	[12]
FE-I3	2003	50 \times 400	18 \times 160	3.5 M	DSM 0.25 μm CMOS, 6M	[13–16]

Table 3: Summary of the ATLAS pixel front-end chips

¹⁾The cascode is a two-stage amplifier composed of a transconductance amplifier followed by a current buffer.

²⁾DMILL technology was developed by CEA, France, and then produced under license by TEMIC Matra MHS

4.2.2 Design

Chip Architecture The readout chip for the ATLAS pixel detector [13, 14] shown in Fig. 7 contains 2880 pixel cells of $50 \times 400 \mu\text{m}^2$ size arranged in a 18×160 matrix. Each pixel cell contains an analogue block where the sensor charge signal is amplified and compared to a programmable threshold by a comparator. The digital readout part transfers the hit pixel address, a hit leading edge (LE) timestamp, and a trailing edge (TE) timestamp to the buffers at the chip periphery. In these buffers a time over threshold (ToT) is calculated by subtracting the TE from LE timestamp. These hit buffers monitor the age of each stored hit by inspecting the LE time stamp. When a hit becomes older than the latency of the L1 trigger ($3.2 \mu\text{s}$) and no trigger signal has occurred, the hit information is deleted. Hits which are marked by trigger signals are selected for readout. Triggered hit data are transmitted serially out of the chip in the same order of trigger arrival.

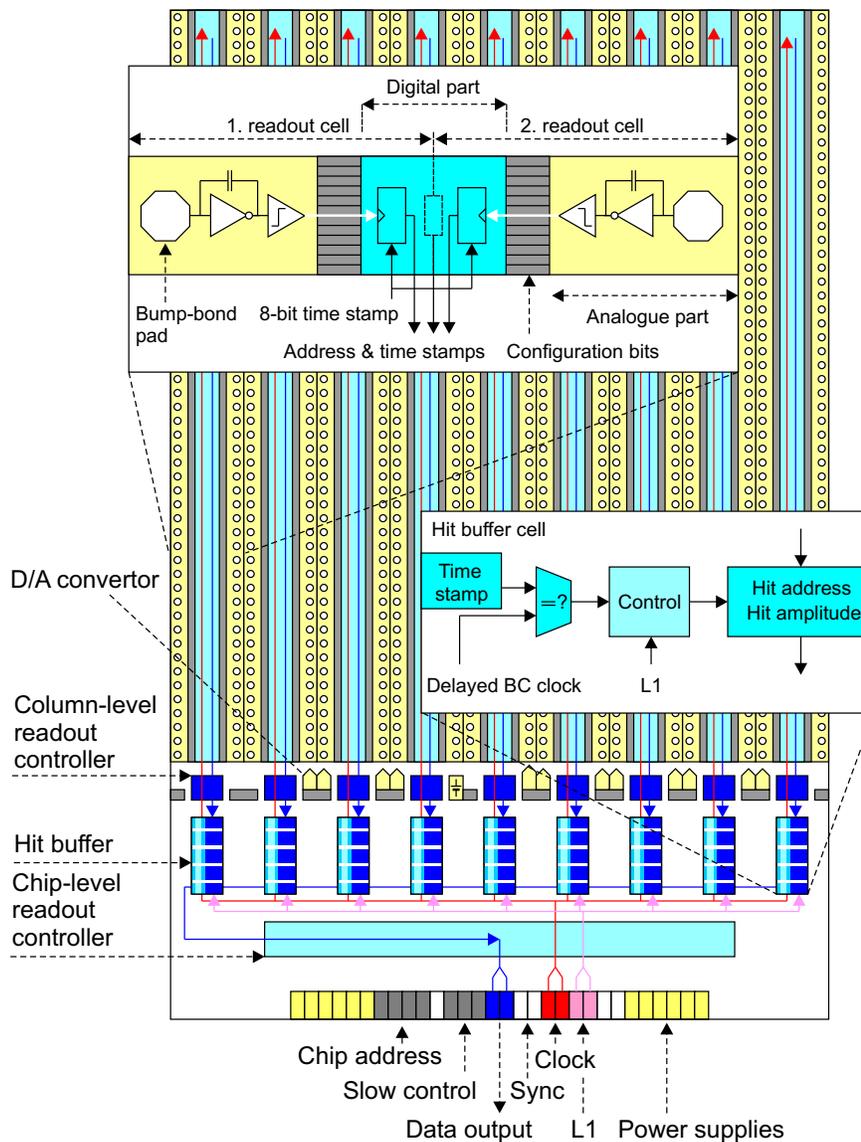


Figure 7: Simplified floorplan of the front-end chip (FE-I3) with main functional elements.

Charge Sensitive Preamplifier The charge sensitive amplifier uses a single-ended folded-cascode topology, which is a common choice for low-voltage and high gain amplifiers. The amplifier is optimised for a nominal capacitive load of 400 fF and designed for negative signal expected from n^+on-n -bulk detectors. Special attention was put in the design of the charge amplifier to the requirement of irradiated sensors, where the leakage current can reach 100nA. The preamplifier has about 5 fF DC feedback design, 15 ns risetime and operates at about $8 \mu A$ bias. Since the input is DC-coupled, a compensation circuit is implemented which drains the leakage current and prevents it from influencing the bias current of the fast feedback circuit, used to discharge the feedback capacitor. The feedback system, shown in Fig. 8 uses two PMOS devices, one (M2) providing leakage current compensation and the other (M1) continuous resetting of the feedback capacitor. // An important property of this feedback circuit is that

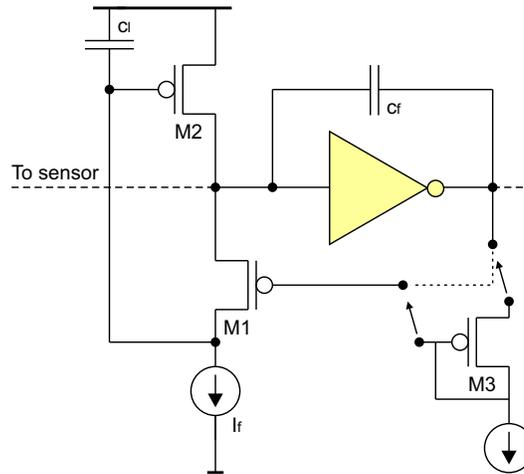


Figure 8: Charge preamplifier: feedback circuit.

the discharge current provided by the reset device saturates for high output signal amplitudes. The return to baseline is therefore nearly linear and a pulse width proportional to the input charge is obtained. The width of the discriminator output, Time-over-Threshold (ToT), can therefore be used to measure the signal amplitude. The duration of the ToT is measured by counting the cycles of the master chip clock. The feedback current is 4 nA for a $1 \mu s$ return to baseline with 20 ke input. The feedback circuit used in FE-I3 has an additional diode-connected transistor M3, which acts as a level shifter so that the DC levels of input and output nodes are nearly equal. It also simplifies the DC coupling between amplifier and the comparator, now described.

Comparator Signal discrimination is made by a two stage-circuit: a fully differential low gain amplifier, where threshold control operates by modifying the input offset, and a DC-coupled differential comparator. The first stage has a bias of about $4 \mu A$ whereas the second uses a current of about $5 \mu A$. In order to make the threshold independent of the local digital supply voltage in each pixel and on the amplifier bias current I_f , a local threshold generator is integrated in every pixel. Seven-bits are used in each pixel to adjust the discriminator threshold.

Pixel Cell Control Logic A complete block diagram of the analogue part with several additional circuit blocks is shown in Fig. 9. Each pixel has several parameters that can be tuned through a 14-bit control register. Those bits are:

- *FDAC 0-2*: 3-bits to trim the feedback I_f current for tuning the ToT response.

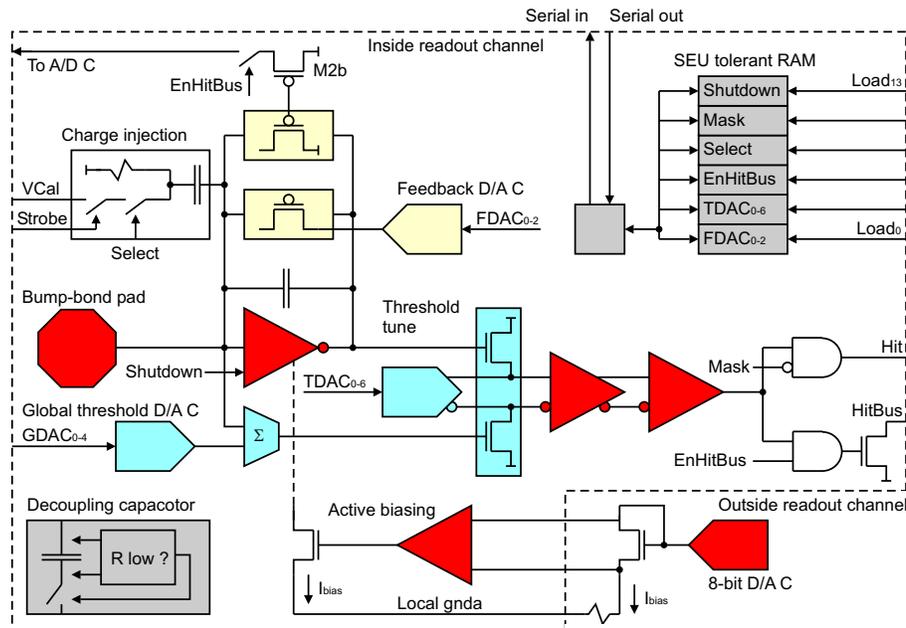


Figure 9: Pixel cell block diagram.

- *TDAC 0-6*: 7-bits to trim the threshold in each pixel.
- *MASK*: the digital output of the analogue part can be switched off locally by setting this bit.
- *EnHitBus*: the digital outputs of all readout channels can be directly observed using a wired OR which is locally enabled with this bit. This bit also controls, through transistor *M2b*, the summing of a current proportional to the feedback plus leakage current in the preamplifier, allowing the monitoring of the feedback current and of the leakage current from the sensor.
- *Select*: enables the pixel for test charge injection. Amplitude is generated from V_{Cal} (Voltage proportional to the injected calibration charge) whereas timing comes from an external *Strobe* signal.
- *Shutdown*: disables the charge amplifier therefore no output is generated from the pixel.

Pixel Cell Readout Logic A block diagram of the column-pair readout is shown in Fig. 10. LE and TE timestamps are temporarily stored in local memories before being transferred to the hit buffers at the chip periphery. A digital circuitry generates two short ($1ns$) strobes at the LE and TE comparator edges, respectively. These signals are used to store the 8-bit Gray-coded time stamp into two memories. The time stamps, generated at the chip periphery, running at 40 MHz are distributed differentially, in order to decrease the digital crosstalk to analogue circuits and sensor electrodes. The complete hit information is available after the TE of the comparator signal and data transfer can start. The time stamp of the LE (8-bits), of the TE (8-bits) and the row number (8-bits) are transferred to the end-of-column (EoC) buffers. Transfer happens by a priority mechanism that selects cells with data starting from the top row. The top most cell with a hit puts the data on the bus and all the cells below it are inhibited. When the cell is read out, it releases the priority encoder bus and the next coming hit is selected and put on the readout bus. The readout speed is limited by the time the priority logic needs to ripple down. Hits can ripple

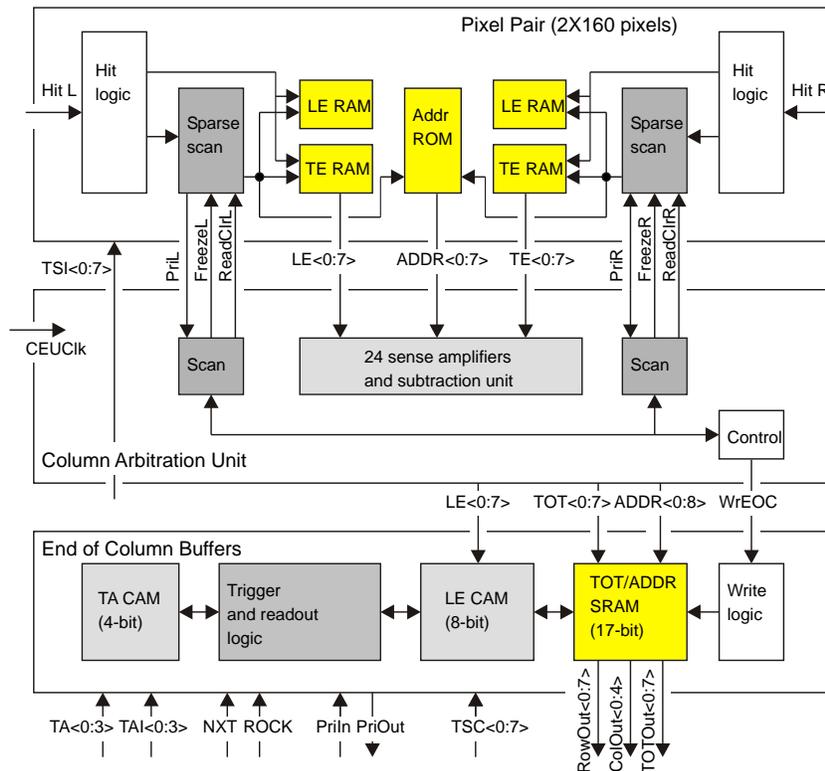


Figure 10: Block diagram of the column-pair readout.

through at programmable speed that is obtained from the 40 MHz clock division. In the actual chip, the maximum speed to transfer a single hit to the EoC is 20 MHz.

Column Readout Controller Readout is column based, and two columns are readout from the same controller. The first task of the controller is the generation of the readout sequence to transfer hit information: LE and TE timestamp, plus pixel row address into an EoC buffer. This operation begins when data is complete, which is after discriminator TE. The transfer of hits from a column pair is synchronized by the Controller end-of-column Unit (CEU), which operates at a speed of 5, 10, or 20 MHz. A total of 64-hit buffers are available for each double-column. The second task is some digital processing of the hit data. Hit information is formatted by the CEU. Formatting includes ToT calculation: subtraction of TE time stamp from LE timestamp. Optionally, a digital threshold may be applied to ToT, a timewalk (time slewing for small charges with respect to high charge) correction may be applied (write hit twice if below correction threshold, once with LE and once with LE - 1), or both. These operations are pipelined to minimize deadtime, but EoC writes cannot occur faster than 20 MHz. Hit information is written to the EoC buffer, and waits there for a corresponding L1 trigger. If a trigger arrives at the correct time, checked using LE timestamp of hit, the data is tagged as belonging to a particular 4-bit trigger number. Otherwise, it is reset and the buffer is freed. Once the chip has received L1 triggers, the trigger FIFO will no longer be empty. This initiates a readout sequence in which the EoC buffers are scanned for the presence of hits belonging to a particular trigger number. If hits are found, they are sent to the output serializer block, which encodes and transmits them to the Module Controller Chip (MCC). After all hits for a given trigger number have been sent, an End-of-Event (EoE) word is appended to the data stream. All of these operations occur concurrently and without deadtime, with all column pairs operating independently and

in parallel.

Event readout from the EoC buffers happens concurrently with the column readout. When the chip-level readout controller starts processing a particular L1 event, it first broadcasts the corresponding L1 readout address to all buffers. All cells with hits waiting for readout compare their stored L1 address with the request value. The readout of the selected L1 hits is controlled by a priority network; which sort them in column and row order.

Chip Level Readout Controller The chip-level readout controller collects hit data from the EoC buffers and sends out of the chip serially. All the hits belonging to the same L1 are grouped together into a single event, and events are transmitted out of the chip in consecutive trigger order. When a L1 trigger arrives, the current bunch crossing time and a buffer overflow bit are stored in a 16 locations deep FIFO memory. This allows the chip to keep track of 16 pending L1 signals. The write pointer of the FIFO is used as the L1 identification, which is sent to the hit buffers. The readout sequence is started as soon as the FIFO receives an L1 trigger. If the L1 priority scan in the hit buffers flags cells with matching trigger numbers, the data of the first cell in the hierarchy is sent to a global data bus where the information is copied to a shift register. The content of the shift register is then transmitted serially. This is repeated until the priority scan shows no more hits. An End-of-Event (EoE) data word, which includes error flags, is then added to the event.

Chip Configuration FE-I3 has 231 global configuration bits plus 14 local bits for each of the 2880 readout channels. The global bits are the settings for eleven 8-bit bias current DACs and for one 10-bit calibration voltage DAC, global threshold bits, the L1 latency, ToT filter thresholds, column enable bits, and others. The configuration is loaded into the chip using a serial protocol running at 5 MHz. This protocol uses three chip input pads: data input, clock and load. Each write operation begins with a 4-bit address, which permits the 16 chips in a module to receive independent configurations. The address of each chip is encoded with wire-bonds during module assembly.

4.2.3 Requirements and Measured Performance

Design requirements come from operation of the pixel detector at high radiation dose, from the time resolution of 25 ns to separate two contiguous bunch crossings, from noise, from minimum operation threshold and dispersion and from the overall power budget. Operation relies on 7-bit adjustment of individual pixel thresholds (tuning). The un-tuned (tuned) threshold dispersion is $\sigma = 800$ (70) electrons equivalent input charge (e). The noise is 160 e and the typical operating threshold is 4000 e , which results in hits $> 5500e$ appearing in the correct 25 ns time bucket (described as in-time threshold) [15, 16]. Neither the dispersion nor the noise depends on the choice of threshold. The tuned thresholds have been observed to re-disperse with moderate radiation dose in prototypes, and it is expected that periodic threshold re-tuning will be needed operation. However, the actual dispersion rate in the real operating environment will need to be measured. An selectable option internally duplicates near-threshold hits in two adjacent time buckets in order to allow recovery of in-time threshold inefficiency. Measurements made on few modules irradiated to 60 Mrad (in excess of the full LHC-life dose) show a negligible tuned threshold dispersion and a 20% increase in the noise, in spite of the very high leakage current (60 nA for normal pixels). For a configured chip the typical digital current is 45 mA at 2 V and the analogue current is 75 mA at 1.6 V for a total power of 220 mW. Chip production was made in batches of 48 wafers. There are 288 chips on each 12-inch wafer. Six production batches were purchased with the 6 wafers from the engineering production run. The total number of wafers is 294. The average wafer probing yield was about 80%. The ATLAS pixel detector contains a total of 27904 front-end chips.

4.3 Module Control Chip (MCC)

4.3.1 MCC History

The prototype sequence leading up to the Module Controller Chip (MCC) is shown in Table 4. The

Chip	Year	# of Std.Cells	# of Trans.	Chip size (mm^2)	Technology
MCC-AMS	Apr 1998	17922	363 000	10.3×6.3	AMS $0.8\mu m$ CMOS, 2M
MCC-D0	Aug 1999	–	–	6.1×3.5	DMILL $0.8\mu m$ BiCMOS 2M
MCC-D2	Aug 2000	13446	328 000	11.9×8.4	DMILL $0.8\mu m$ BiCMOS, 2M
MCC-I1	Nov 2001	33210	650 000	6.38×3.98	DSM $0.25\mu m$ CMOS, 5M
MCC-I2	Feb 2003	67919	880 000	6.84×5.14	DSM $0.25\mu m$ CMOS, 5M
MCC-I2.1	2003	67919	880 000	6.84×5.14	DSM $0.25\mu m$ CMOS, 5M

Table 4: Summary of the ATLAS pixel MCC chips

very first version of the chip, submitted in 1998, was rad-soft and was made in AMS $0.8\mu m$ CMOS technology [17]. This version of the chip had been extensively used when building rad-soft modules. This technology was chosen as it was very close to the $0.8\mu m$ BiCMOS DMILL technology which, at the time, was the chosen rad-hard technology for the ATLAS pixel detector.

A first prototype of the rad-hard chip (MCC-D0) was built in 1999. It contained only one Receiver, but all the remaining circuitry was implemented providing a good test of the DMILL technology. The final version of the chip (MCC-D2) was submitted in Aug 2000. The chip worked fine but an unacceptable low yield, both in MCC-D2 and FE-D2, ruled out this technology.

At this point the MCC was ported to the DSM $0.25\mu m$ CMOS technology and the MCC-I1 chip was submitted in Nov 2001. A new version of the chip, MCC-I2, was built in 2003 in order to provide better Single Event Upset (SEU) hardening to the chip. It turned out that the chip had a small bug that could be corrected modifying only one metal line. Six additional wafers, containing the correction in the layout, were produced in 2003 leading to the final MCC-I2.1 chip.

4.3.2 Design

This section briefly describes the actual implementation of the production MCC chip, labeled MCC-I2.1. A simplified block diagram of the MCC internal architecture is shown in Fig. 11. The MCC has three main system tasks: (1) loading parameter and configuration data in the FEs and in the MCC itself, (2) distributing of timing signals such as bunch-crossing, L1 trigger and resets, and (3) reading out of the FE chip and event building.

System configuration The FE chips and the MCC must be configured after power-up or before starting a data-taking run. It is possible to write and read to all the MCC registers and FIFOs. This is used to configure, to read status information or to test the functionality of the chip. For this last function we provide a special set of commands that allows one to write simulated events into the FIFOs and two to run the Event Builder with the stored values in order to check the complete functionality of the chip. Once the MCC is embedded in the pixel detector, it will be important to test if the event building works with known simulated events. Global FE chip registers and parameters in each of the pixel cells have to be written and read back through the MCC.

Trigger, reset and timing The second task the MCC has to deal with is the distribution of L1 triggers, resets and calibration/timing signals for the FE chips. In *Data Taking* mode, each time a L1 trigger command is received by the MCC the Trigger, Timing & Control (TTC) logic issues a Trigger to the

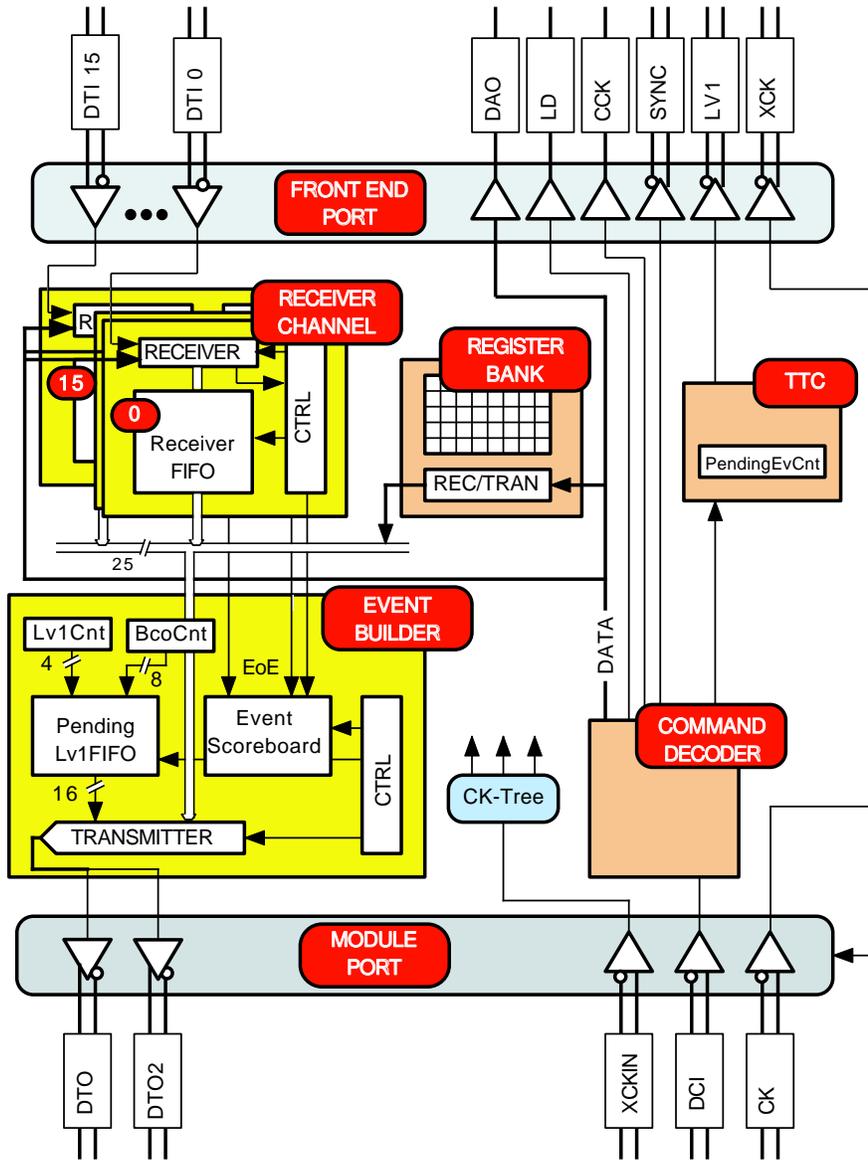


Figure 11: MCC block diagram.

FEs, as long as there are less than 16 events still to be processed. In case of an overflow the L1 trigger is not generated by the MCC and the corresponding event is lost. The information is sent to the ROD together with the number of missing events in order to keep up with event synchronization. In addition to the triggers, the TTC logic generates a hierarchy of reset signals that can be applied either to the MCC or to one or more FE's.

The last function of the TTC logic is the ability to issue calibration strobes to the FEs. This is used to calibrate the FE analogue cells on a pixel by pixel basis.

Event building The read-out architecture that was chosen for the pixel detector is a data-push architecture with two levels of buffering: EoC buffers in the FE chips and 16 individual 128×27 -bit depth FIFOs (ReceiverFIFO) at the MCC inputs.

Event readout and building is by far the most complicated task and it requires that most of the chip area to be implemented. Data received from the FEs, in response to a L1 trigger, are deserialized and buffered into 16 FIFOs, one FIFO for each receiving FE line. These FIFOs are used to derandomise the 16 data rows from the FEs and are used by the event builder to extract ordered hits and to prepare them for transmission out of the pixel module. Event building is performed by two concurrent processes running in the MCC. The first (Receiver) deals with the filling of the 16 input FIFOs with data received from the corresponding FE chip, while the second (Event Builder) extracts data from the FIFOs and builds up the event. Each FE sends data as soon as they are available with two constraints. Event hits must be ordered by event number and for each event an end-of-event (EoE) word is generated. EoE is also sent for the case of an empty event to maintain the event synchronization.

The event transmitted to the ROD is organized by the Event Builder process on an event-by-event basis, instead of a hit-by-hit basis. If the FIFO becomes full while storing incoming hits, all subsequent hits are discarded and only the EoE word is written into the FIFO. In this case, a truncated event tag will be stored in the ReceiverFIFO and then recorded to the MCC output data stream. The mechanism insures that reconstructed events are not corrupted by FIFO overflows.

As soon as the Event Builder finds that an event is completely received from all of the 16 FEs (Event Builder knows from the Scoreboard about the existence of complete events) it starts building up and transmitting the event. The first information written to the output data stream is the bunch crossing identifier (BCID) and the L1 identifier (L1ID). At this point the Event Builder starts fetching data from the ReceiverFIFOs, until it finds an EoE in the data. Once the Event is finished a Trailer word is sent out in order to inform the ROD that the Event has ended.

I/O Protocols Several serial protocols were defined for communication to/from ROD/MCC and MCC/FE. All protocols that are active during data taking use only LVDS type signals, while signals used in the configuration time have single-ended CMOS to reduce the number of interconnection lines. Communications from the ROD to the MCC use a 40 Mb/s data line (Data Command Input - DCI) validated by the rising edge of the 40 MHz clock (CK).

The MCC to ROD link may use 40, 80 or 160 Mb/s data rate. For the case of 40 Mb/s a new bit is transmitted at every rising edge of the CK. For the 80 Mb/s, bits are sent at both CK transitions. Finally for 160 Mb/s, both lines and clock edges are used (this can be considered as a 2-bit wide serial link). Only event read-out uses the two higher bit rates. Read-out of configuration data is always at the 40 Mb/s rate. Data passing from the MCC to the ROD improved robustness by providing a bit-slip safe Header and adding synchronization bits after known numbers of clock cycles.

Communications from MCC to FE chips use a serial CMOS data bus (Data Address Output - DAO), a CMOS control line (Load - LD) and a 5 MHz validation CMOS clock (Control Clock - CCK). Both configuration and event data from the FE to the MCC are transmitted using 16 individual LVDS serial links (Data Input - DTI).

Special care has been placed in the implementation of the Data-Taking protocols in order to minimize the effect of possible Single Event Upset (SEU) events. In particular, while in data taking mode there are only two possible 5-bit commands: trigger and exit data-taking mode. All permutations of the trigger command obtained by flipping one single bit are also interpreted as a trigger command with the correct timing.

4.3.3 Performance

The design requirements need to address the pixel detector operation at high radiation dose, the time resolution of 25 ns separating two contiguous bunch crossings, the expected bandwidths at the highest luminosity, the L1 trigger rate of 100 kHz and the number of FE chips that are controlled by a module.

The 16 FIFO's present in the MCC were designed in order to cope with expected data rate of the FE chips operating at full luminosity with a L1 trigger rate of 100 kHz. Special care has been put in making a Single Event Upset (SEU) robust design, due to the harsh radiation environment that the pixel detector will have to sustain (50 Mrad in three years of operation for the innermost pixel layer). This problem has been addressed using either triple redundancy majority logics or error detection and correction schemes. We irradiated several modules up to the full LHC-life dose, continuously reading out data during irradiation. From studies of the SEU, we can extrapolate to stable operation at the LHC without a significant loss of configuration data due to bit-flip in the memory elements.

For a configured chip the typical digital current is 145 mA at 2.0 V, and a clock frequency of 40 MHz for a total power of 290 mW. All MCC-I2.1 chips were produced in a single batch of 6 wafers. The number of potentially good chips per wafer is 536. The measured yield was of 83%, providing a total of 2666 good chips. A total of 1744 chips are used in the ATLAS pixel detector.

4.4 Optical Communication

4.4.1 Optolink Architecture

The communication between the detector modules and the off-detector electronics is made via optical links. This has been selected to obtain electrical de-coupling and minimise the material budget. The architecture was inherited from the ATLAS SCT [18]. Modifications were made to adapt it to the data-rates, modularities and radiation hardness needs of the pixel detector.

A block diagram of the optical-link system architecture is shown in Fig. 12. The two main com-

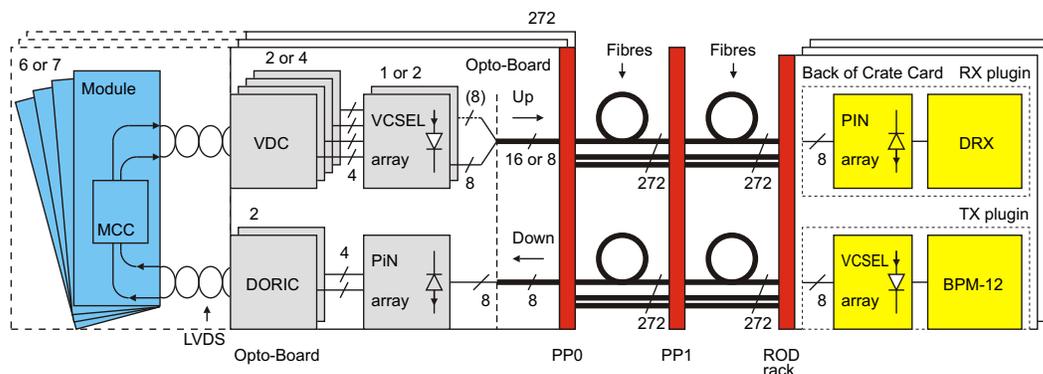


Figure 12: Optical link System Architecture

ponents in the optical link system are the opto-board, on the detector side, and the Back of Crate Card

(BOC), on the opposite end. To keep the material budget low, to accommodate fiber routing requirements, to control radiation exposure, and to permit the use of optical arrays, the opto components and the related receiver/driver ICs were not installed into the detector modules. The components have been put instead on opto-boards at Patch Panel 0 (PP0 - see section 7), at a distance of about one meter from the modules and at relatively large radius in the Pixel Support Tube (PST).

The transmission of the signals from the detector modules to the opto boards uses LVDS electrical connections. These serial connections link the MCC with VCSEL Driver IC (VDC) and the Digital Optical Receiver IC (DORIC) sited on the opto-boards. DORIC and VDC designs were derived from the SCT project; but have been adapted to survive the higher radiation dose seen in the pixel detector. These chips have been fabricated on the same silicon wafers used to produce the MCC chips.

The communication with each detector module uses individual fibres: one for down-link and one or two for up-links. Trigger, clock, commands and configuration travel on the down-link, while event data or configuration read-back data travel on the up-link(s). On the down-link bi-phase mark (BPM) encoding is used to send a 40 Mb/s control stream on the same channel as the 40 MHz Bunch Crossing (BC) clock. Decoding of the BPM channel within the DORIC recovers both the data stream and the clock signal. The use of individual links for every module permits the adjustment of the timing, used to associate the hit to the bunch crossing, by changing the delay of the transmitted signal with respect to the phase of the LHC machine reference clock received in the BOC.

The readout bandwidth required to extract the hits from the detector modules depends on the LHC instantaneous luminosity, on the L1 rate and on the distance between the module and the interaction point. Simulation of the readout architecture with generated physics events [17] shows that a bit rate of 40 Mb/s for the Layer-2 modules, 80 Mb/s for the Layer-1 or Disk modules and 160 Mb/s for the B-layer modules are needed to keep the number of lost hits due to bandwidth saturation sufficiently low. The data transmitted in up-link are encoded in non-return-to-zero (NRZ) format. Electrical to optical conversion happens in the opto-boards on the detector side and in the RX- and TX-pluggings in the BOC.

There are two flavours of opto-boards: Disk/L1/L2-boards (D-board) with 8 down-link and 8 up-link channels and B-layer-boards (B-board) with 8 down-links and 16 up-links. The B-boards use two 80 Mb/s channels to obtain the aggregated bandwidth of 160 Mb/s needed for the B-layer modules. Because of the modularity of staves (13 modules) and of sectors (6 modules) D-boards use either 6 channels for the disk-sectors or 6/7 channels for the half-staves in Layer-1 and Layer-2. B-boards, instead, are used in the B-layer staves where two uplinks per module are needed.

In the off-detector part of the links, one BOC exists for each ROD. BOCs come with a variety of hardware options that are implemented by equipping the card with a larger or smaller number of optical receiver (RX-plugin) or transmitter (TX-plugin) plug-ins. Each plug-in, in principle, can serve up to 8 modules, but, in practice, only 6 or 7 are used due to the modularity of the detector. Each BOC has space for 4 TX-pluggings and 4 RX-pluggings. BOCs come with 4 TX and 4 RX where the maximum bandwidth requirement is of 40 Mb/s, with 2 TX and 4 RX for 80 Mb/s and with 1 TX and 4 RX, for 160 Mb/s. Two full custom chips have been designed by the SCT collaboration and used in the optical plug-ins; they are the DRX (12-channels Data Receiver ASIC in the RX) and the BPM-12 (12-channels Bi-Phase Mark encoder ASIC in the TX). In the BOC there is also the optical S-Link interface used to send the ROD output to the ATLAS Readout Buffer (ROB) units, which are the next level up in the event readout chain.

4.4.2 opto-board

The opto-board is the opto/electro-interface on the detector side. It consists of a beryllium-oxide (BeO) printed circuit board measuring $2 \times 6.5 \text{ cm}^2$. As discussed in Section 4.4.1 two flavours of opto-boards (D-boards and B-boards) exist and six or seven detector modules are connected to them. The D-boards are equipped with one PiN diode array and one VCSEL-array (Vertical-Cavity Surface-Emitting Laser),

while the B-boards have a second VCSEL-array. Each opto-board loads two 4-channel DORIC chips, whereas two and four 4-channels VDC chips are loaded in the D-board and B-boards, respectively. The optopack, which holds the PiN/VCSEL arrays and the connector to plug the optical fibres, has a custom design in order to fulfil requirements that it be low mass, non-magnetic and radiation tolerance. The total number of opto-boards in the detector is 288. This is more than the minimum 272 (44 B-boards and 228 D-boards) needed to read out the detector in order to have spares available to recover from problems during integration. In the end only one spare board was used. The remaining spares remain mounted in the detector, but not connected.

PiN diode array Arrays of silicon PiN diodes are used to receive the data sent by the VCSELs. Epitaxial silicon PiN diodes are used because the intrinsic layer provides a thin active layer allowing for fast operation at low PiN bias voltage. The active area of each individual PiN diode is circular with a diameter of $130\ \mu\text{m}$ and the depth of the intrinsic region is $35\ \mu\text{m}$ [18].

DORIC The DORIC integrated circuit has the function of amplifying the optical signal detected in the PiN diode and of reconstructing the clock and data channels from the BPM coding. Data and clock are transmitted, using LVDS signal levels, to the MCC. Each DORIC chip contains four identical channels. The specification for the current from the PiN diode is in the range of $40\ \mu\text{A}$ to $1\ \text{mA}$. The requirements for the extracted clock are a duty cycle of $50 \pm 4\%$ and a time jitter better than $1\ \text{ns}$. The DORIC has been designed to have a bit error rate better than 10^{-11} after a radiation life dose. This condition is obtained with a PiN-diode bias current of less than $20\ \text{mA}$. The PiN diode current amplifiers use a single ended scheme [19]. This design solution avoids the chip having to see at its inputs the diode bias voltage, which is higher than the rating for the integrated circuit technology. The DORIC must withstand up to $10\ \text{Mrad}$ over the 10 years of ATLAS operation. It is, therefore, implemented in the same proven ($0.25\ \mu\text{m}$) CMOS technology as used for FE, MCC and VDC.

VDC The VDC converts the LVDS input signal, received from the MCC, into a suitable single-ended signal to drive the VCSELs in a common cathode array configuration. The VDC chips come with four channels and drive one half of the VCSELs array. An external current used to drive the VCSEL operates up to $20\ \text{mA}$. The nominal current to operate the VCSEL is $10\ \text{mA}$. A standing (dim) current of $\sim 1\ \text{mA}$ is provided to improve switching speed in the VCSEL. The dim current is remotely controlled by an external voltage. The requirement for the rise/fall time (20 to 80 %) is in the range of 0.5 to $2.0\ \text{ns}$, where $1.0\ \text{ns}$ is nominal. A further requirement, relevant to reducing the pick-up noise pertains to the constant power consumption of the VDC, that is independent from VCSEL being bright (on) or dim (off). A voltage ($V_{I_{set}}$), remotely controlled, determines the current I_{set} that sets the amplitude of the VCSEL current (bright minus dim current).

VCSEL array Vertical-Cavity Surface-Emitting Laser (VCSEL) arrays are used to transmit the data optically. The main advantages of VCSELs are that they provide large optical signals at very low currents and have fast rise and fall times. In order to maintain low the laser threshold current, VCSELs use ion-implants to selectively produce a buried current-blocking layer to funnel current through a small area of the active layer. The VCSELs [18] used in the pixel and SCT systems have an oxide implant to achieve the current confinement, which is becoming the standard VCSEL technology as it produces lower current thresholds at higher bandwidth. VCSELs are produced in arrays of 8 diodes. The typical fibre coupled power per channel is greater than $1\ \text{mW}$ at a drive current of $10\ \text{mA}$. This optical power at $10\ \text{mA}$ is sufficient to give a noise immunity of $6.2\ \text{dB}$. Using a slightly higher current is possible, if one adds another $1.8\ \text{dB}$ of noise immunity. The down-link, where the current is not a critical issue, can profit

from this improved margin corresponding to a higher immunity to SEU and to Bit Error Rate (BER). One mW of optical signal ensures a BER better than 10^{-9} .

4.4.3 Back of Crate Card (BOC)

Each BOC is connected to one ROD through the crate back-plane. The BOC has two functions: interface between ROD and opto-links and distribution of the timing to the on- and off-detector electronics. Each BOC receives a system clock signal and redistributes it to the pixel detector modules and ROD. Each detector module needs a precise phase adjustment of its 40 MHz clock relative to the bunch-crossing time reference. The adjustment of this phase can be done for each module independently. This is made by an ASIC (PHOS4) that contains four programmable delay channels, which are programmable in the range of 0 to 25 ns. The PHOS4 chip is also used to adjust the sampling clock that controls data received from the pixel modules. The opto-electrical conversion and the connection to the fibres is located in two card plug-ins: TX-pluggings and RX-pluggings, respectively, for transmission and reception of optical data. The TX-plugin has an 8-channel VCSEL array and a BPM-12 ASIC. The RX-plugin has an 8-channel PiN diode array and a DRX ASICS.

DRX The DRX ASIC amplifies, discriminates and converts the signal from the PiN diode into an LVDS signal. The comparator is DC coupled and the threshold can be controlled over a current range up to $255 \mu\text{A}$ by an external voltage reference generated by a DAC. The DRX chip was originally designed for the ATLAS SCT detector and contains 12 channels. Only 8 channels per chip are used in the pixel BOC.

BPM-12 The BPM-12 ASIC does the encoding of clock and data in the Bi-Phase Mark format that is used in the fibre optic transmission. This chip was originally designed for the SCT detector and only 8 of the 12 channels are used for the pixels. A critical specification for this component is to have a short delay between input signals and encoded outputs because it is added to the overall L1 trigger delay. The measured delay value is 60 ns.

4.4.4 Opto-fibres

The connection between the BOC and the opto-boards is made with optical fibres. Two different kinds of fibres are used, Stepped Index Multi-Mode fibres (SIMM) and GRaded INdex multi-mode fibres (GRIN). SIMM fibres have been tested to be radiation tolerant but have lower bandwidth per unit length than GRIN fibres [20]. To optimise the bandwidth and radiation tolerance, splicing of 12 m long SIMM and 70 m long GRIN fibres has been used. The fibres are ribbonised into 8-way ribbons and 8 ribbons make an optical cable. The 12 m length of the SIMM fibre is segmented by a MT16 connector at ~ 2.5 m from PP0 (at PP1). A total of 84 cables have been installed.

4.4.5 Optolink Performance

The selection and qualification of the components to be used in the optolink system was done by extensive laboratory tests, irradiation campaigns and system measurement in test beams. From the measurements made on single components or parts of the system, we predict a good behaviour for the optolinks over 10 year of operation at LHC [19–23]. The measurement of the bit-error-rate in optolink ring-loops running at 40 Mb/s (80 Mb/s) gives an upper limit $BER < 1.45 \times 10^{-14}$ ($BER < 3.62 \times 10^{-14}$). In fact no single errors were found [24]. The method to adjust the timing in the BOC to time the pixel detector with a bunch crossing is reported in [25]. Using the current procedure, automatic tuning of the optolink

parameters (the system laser forward currents, PiN-diode photo-current thresholds, etc.) is achieved in (extrapolated to the whole detector system) under 10 min.

4.4.6 Production of Optolink Parts

During the qualification test of production components it was observed that several batches of VCSELs had a large output light power spread varying with temperature. Many VCSELs give a power, coupled to the fibre, below the specification requirement ($350 \mu\text{W}$) at the nominal operating temperature inside the pixel detector (-7°C). To overcome the problem it was decided to add a temperature regulation of the optboards, giving the possibility to operate at 20°C . One VCSEL and one PIN arrays failed during detector integration. In each case single channel of the array ceased to function. The cause of these failures was not determined. In both cases the affected modules were recovering by switching to a spare opto board in one case and by moving only one module to an unused (7^{th} channel of a board serving only 6 modules) in the other.

Optical fibres, fabricated and assembled by external companies, have been tested during production by measuring light coupling and attenuation. Two out of 86×8 8-way ribbons showed failures. Fibres are tested again after installation with a Time Domain Reflectometer and replaced by spares in case of failure.

4.5 Data Acquisition System

The pixel detector Data Acquisition System (DAQ) has been designed following the specification of the ATLAS global DAQ architecture [26].

4.5.1 Architecture overview

The off-detector readout architecture of ATLAS consists of two parts: a sub-detector specific part, where the Readout Buffers (ROD) are the main building blocks, and an ATLAS common design that is referred as the Read Out System (ROS) [27].

The pixel ROD [28] is a 9U-VME module. The ROD handles the data transfer from the on-detector electronics on one side to the ROS system on the other side. Data from the detector arrive at the RODs through the BOCs. Data passes through the BOCs and is then received at the ROS by custom designed interface modules. The ROS is a PC based system. These PCs temporarily store readout events into their memory and transfer only those accepted by the L2 trigger to the next level up in the readout chain.

ROD modules are plugged into ROD crates. There are 9 crates with up to 16 ROD modules per crate. In total, there are 44 modules or 3 crates for the B-layer, 38 modules for Layer-1 plus 28 modules for Layer-2 or 4 crates and 24 modules or 2 crates for the disks. A Trigger, Timing & Control Interface Module (TIM) [29–31] and a Single Board Computer (SBC) [32] complete the ROD crate. The TIM is the interface to the Trigger System. The DAQ software running in the SBCs controls the modules in the ROD crate. There is no event traffic on the ROD VME-bus during normal data-taking; data are routed directly from the ROD to the ROS PCs [27] via fast optical links (S-Link). The VME-bus is, instead, heavily used during calibration of the pixel detector. RODs are controlled, via VME bus, by the SBC which also acts as interface to the global DAQ system.

Calibration data are treated differently from collision data. The procedure to calibrate the pixel detector consists of a sequence of injections of a known charge into the pixel's front-end amplifiers. The response of each pixel is measured as a function of the injected charge and of other parameters (thresholds, preamplifier feedback currents, trigger delay) that can be varied during the calibration procedure. The typical result of a calibration sequence consists of a set of occupancy histograms corresponding to different values of the scanned parameters. In order to achieve maximum precision, it is important to

extract data from the FEs at the maximum speed supported by the detector links. This makes it difficult to extract calibration data using the normal data path, as the read-out chain from the ROS to the Event Builder is designed to transfer only L2-trigger accepted events, while the detector links are designed to support the full L1 trigger rate. For this reason, during calibration runs, the ROD decodes the data stream sent by the front-end electronics, fills occupancy histograms and stores them in memory. The histograms are then extracted via the VME bus by the SBC and set to an analysis farm for further manipulation and archiving.

Single Board Computer (SBC) The Single Board Computer is a commercial VP-315³⁾ 6U VME card with a Pentium-M⁴⁾, having 1.6 GHz clock and 1 GB memory. The card uses a Universe II⁵⁾ PCI-VME bridge. It has three gigabit-ethernet interfaces, of which two are used, one to connect to the ATLAS control network and the second to the analysis farm, where histograms generated in the ROD are collected. Up to 40 MB of internal RAM memory is used to cache the configuration data needed in the pixel detector modules for a complete crate of RODs. The configuration data, cached in the SBC memory, are stored offline in an Oracle database⁶⁾ server. The memory is also used as a transfer buffer for the histograms moved from RODs to analysis farm.

Trigger, Timing & Control Module (TIM) The TIM is the interface between a ROD crate and the ATLAS trigger system. It receives a TTC fibre-link from a Local Trigger Processor (LTP), carrying LHC bunch crossing (BC) and orbit signals, the trigger signals like Level 1 Accept (L1A) and the trigger type, control/synchronisation signals like event counter reset (ECR) and synchronisation (SYN). These signals are distributed to the RODs via a custom backplane installed in the lower part of the VME crate. On the same backplane the busy signals generated by the RODs go to the TIM. The TIM makes a collective ROD card Busy and sends a signal to the LTP. The LTP on reception of a Busy signal stops the L1A to the detector electronics, thus allowing the front-end and ROD buffers to be emptied. Several features are implemented in the TIM to operate on the trigger signal. Programmable delay on distributed triggers, generation of trigger bursts and generation of strobe signals having a fixed delay from a L1A. Moreover, the TIM can be used as a local trigger generator with programmable rate. This has been very useful for studying ROD and DAQ behaviour on simulated event rates.

Read Out Driver (ROD) The structure of the ROD is outlined in Fig. 13, Three main sections of the design are the control path, data flow path, and the Digital Signal Processing (DSP) Farm. The control path section consists of two Xilinx Field Programmable Gate Arrays (FPGA) and a Texas Instruments Fixed Point Digital Processor (TI 320C6201 operating at 160MHz with 32MB SDRAM). The Program Reset Manager (PRM) FPGA functions as a VME slave controller, allowing read and write access to all ROD and BOC registers and a configuration controller for all of the data path FPGAs. To enable the users to easily upgrade the firmware on the ROD, the PRM FPGA allows VME access to an on-board Flash memory chip that stores the configuration data for all of the data flow path FPGAs. The Master DSP receives commands and transmits replies to the VME host and coordinates the configuration, calibration and data-taking modes of the ROD. The ROD Controller FPGA is used in the control path as an interface for the Master DSP to the DSP farm, the BOC, and all of the internal ROD registers in the data flow FPGAs. It also controls all of the required, data flow path specific, real-time functions on the ROD, including serial transmission of commands to the FE modules (two independent command streams can be sent to two modules or group of modules), calibration mode trigger generation, and transmission of

³⁾From Concurrent Technologies Corporation, <http://www.ctc.com>

⁴⁾From Intel Corporation, <http://www.intel.com>

⁵⁾From Tundra Semiconductor Corporation, <http://www.tundra.com>

⁶⁾From Oracle Corporation, <http://www.oracle.com/>

Figure 13: Block diagram of the ROD.

TIM generated triggers and fast commands. In summary, these are the main actions performed by the control path block:

- full control of ROD reset and FPGA configuration;
- receives and executes command from the SBC via VME;
- receives module configurations via VME and stores them in Master DSP memory;
- transmits configuration data to the modules;
- control of calibration procedures, transmitting triggers and configuration data to FE modules;
- control of FE module data histograms;
- propagation of trigger commands from the TIM to the FE modules.

The structure of the ROD Data Flow Section is outlined in the block diagram of Fig. 14. The data flow section receives serial data from the FE modules, packs the individual module fragments into a single ROD fragment and sends it to the ROS via a custom designed optical link called the S-Link. Four blocks can be identified: the Input Link Interface, the Formatter, the Event Builder and the Router. Normal event data flows through the ROD via the Input Link Interface, which leaves the data unchanged. It can, however, trap the serial data stream in FIFOs (used in module configuration or to trap an event for diagnostics). The FIFOs can also be loaded with events for analysis by the ROD for diagnostics. After the Input Link Interface, the Event data enters the Formatters. The Formatters convert the serial data streams to parallel format, and fill the de-randomizing buffers used to queue events for transmission to the Event Fragment Builder (EFB) FPGA. An event is transmitted from the Formatters to the Event Fragment Builder after the Controller FPGA sends a command notify that a Level 1 Accept has been sent to the modules. The ROD Event Fragment is constructed in the EFB using the ATLAS Event ID data that was transmitted from the controller FPGA. In normal data taking, the primary source of the

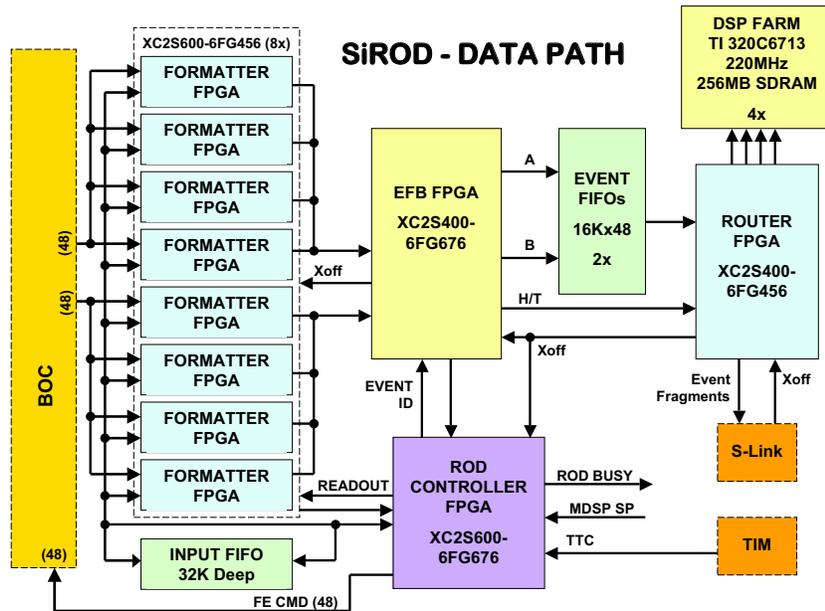


Figure 14: Block diagram of the ROD Data Flow Section.

ATLAS Event ID data is the TIM with the ROD providing some additional information. After the header and mode information is sent to the EFB the ROD Controller FPGA issues one token to the Formatters and event data is pushed to the EFB. The EFB checks LIID and BCID values and records errors. It also records any errors that were decoded or flagged by the Formatters. The event data is then stored in 16K de-randomizing FIFOs (two each). There are two identical engines in the EFB transferring data at up to 40MHz (total bandwidth 80 MHz). When an event is ready (header, data body and trailer in the FIFOs) it is transmitted to the Router. The Router has two main functions. The first one, that is the main physics data path, is to transmit 32 bit data words to the S-Link at 40 MHz. If the S-Link is receiving data faster than it can transfer to the ROD, the S-Link can assert Xoff to apply back pressure to the ROD data path. When back pressure is applied, read out of data from the EFB FIFO is stopped. When the EFB memories are almost full back pressure is applied to the Formatters. This will stop event data transmission from the formatter link FIFOs. The second function of the router is to trap data for the DSPs. This is performed with no effect on the S-Link data during normal running. When the ROD is in calibration mode the DSPs can assert back pressure to pause the ROD data flow.

Finally, the ROD is equipped with four Slave DSP processors (TMS320C6713) with 256 MB memory each. They are connected to the Router FPGA from which they can sample the produced ROD fragments. Different tasks can run on the DSP processors to analyze captured events: monitoring task, used during normal data taking to compute average occupancy and detect noisy pixels or data transmission errors. Calibration tasks accumulate histograms during the multi-dimensional scan procedure and perform an analysis in order to reduce the data volume to be transferred to the SBC. During data taking the DSPs are spying the data-flow at the maximum possible rate without introducing dead time or applying back pressure to the data flow path. During calibration, on the other hand, the slave DSPs must analyze all the fragments, so they actually represent the most important limiting factor for the data rate. For this reason the code of the calibration task must be optimised, making use in the most efficient way of the 128 KB internal DSP fast memory to fill the occupancy histograms.

4.5.2 ROD Crate Software and Calibration Analysis Farm

The ROD Crate software is the interface between the ATLAS Run Control and the pixel detector DAQ. Its structure is outlined in Fig. 15.

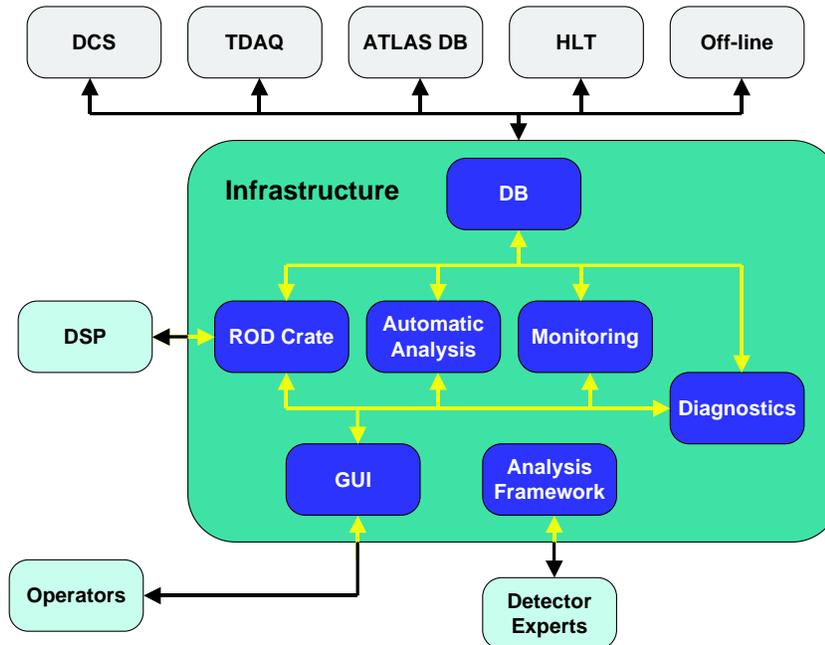


Figure 15: ROD software architecture.

For each ROD in the crate, a ROD Interface thread is created. This interface give access to the basic functionalities that an external applications can perform on the modules using the ROD. The implemented functions range from very basic commands (like ROD module reset and configuration) to complicated scan procedures. The ROD software interfaces are based on Remote Procedure Calls (RPC). They use a Common Object Request Broker Architecture (COBRA) layer called Interprocessor Communication (IPC) which is used in most ATLAS DAQ applications. These interfaces can be accessed either locally in the ROD, from another process running in the SBC, or from a process running on a remote CPU. Only one application at the time can be allowed to access a given ROD; for this reason, each SBC runs a Crate Broker. Each process accessing a ROD must first ask the Crate Broker, verify if the requested resource is free and allocate it. Only at this point is access to the ROD Interface granted. The last element of the ROD Crate software is the Run Controller. This process is a local receiver of the commands issued by the central ATLAS Run Control.

During normal data taking, the ROD Crate Run Control allocates all the ROD Interfaces and executes the transitions (INITIALIZE, CONFIGURE, START, STOP) as indicated by the global Run Control. During calibrations, the Run Control disconnects the RODs, which are then controlled by a Calibration Console, controlling the calibration procedure. The interface/broker mechanism gives the possibility to run a calibration or a debugging session on a ROD while the others are taking data. Occasionally the amount of data produced during a calibration may be too large to fit to the SBC memory. The histograms are then immediately moved (again using IPC) from the SBC to a remote analysis farm, which takes care of the final data analysis, of the generation of a new configuration set based on the tuning/calibration procedure, and of archiving the results. In this way the memory of the SBC is not saturated, and a new scanning procedure is immediately started, while the analysis farm is analyzing the previous data set.

4.6 Detector Control System (DCS), Power Supplies, and Interlock System

The operation of the pixel detector modules and of the on-detector opto-components requires a complex power supply [33] and control system [34, 35]. The following supplies are required at module and opto-board level:

- V_{DDA} : analog low-voltage supply for the FE chips;
- V_{DD} : digital low-voltage supply for the FE chips and the MCC;
- V_{DET} : high-voltage supply to bias the sensor;
- V_{VDC} : low-voltage supply for the VDC and DORIC chips;
- V_{PIN} : PiN diode bias voltage;
- V_{ISET} : digital voltage to to adjust the VCSEL bias;

Electrical budget request for pixel modules and opto-boards is summarised in Table 5. The adjustment

Supply Type	Supply Voltage (V)	Supply Current (mA)	Nominal Voltage (V)	Nominal Current (mA)	Nominal Power (mW)	Worst Voltage (V)	Worst Current (mA)	Worst Power (mW)
Module								
V_{DDA}	10	1500	1.6	1100	1760	2.1	1300	2725
V_{DD}	10	1200	2.0	750	1500	2.5	1000	2500
V_{DET}	600	2	1.6	600	1	600	2	1200
					<i>Module total</i>			3860
D-board								
V_{VDC}	10	800	2.0	280	560	2.5	490	1225
V_{PIN}	20	20	5.0	–	–	20	20	400
V_{ISET}	5	20	1.0	–	–	2	20	60
					<i>D-board (Disk/Layer-1/Layer-2) total</i>			1685
B-board								
V_{VDC}	10	800	2.0	420	784	2.5	770	1925
V_{PIN}	20	20	5.0	–	–	20	20	400
V_{ISET}	5	20	1.0	–	–	2	20	60
					<i>B-board (B-Layer) total</i>			2385

Table 5: Specifications for module and opto-board power supplies.

of the operation conditions of the system requires a large modularity. Robust software packages are used to monitor and control the hardware of the large system. There is, in addition, an independent interlock system that takes care of safety for the equipment and human operators.

4.6.1 The Hardware of the DCS

The scheme of the powering, control and interlock system is shown in Fig. 16. The main components under the pixel DCS are:

- the power supplies to operate the sensors, the front end chips and the opto boards;
- the Regulator Stations;

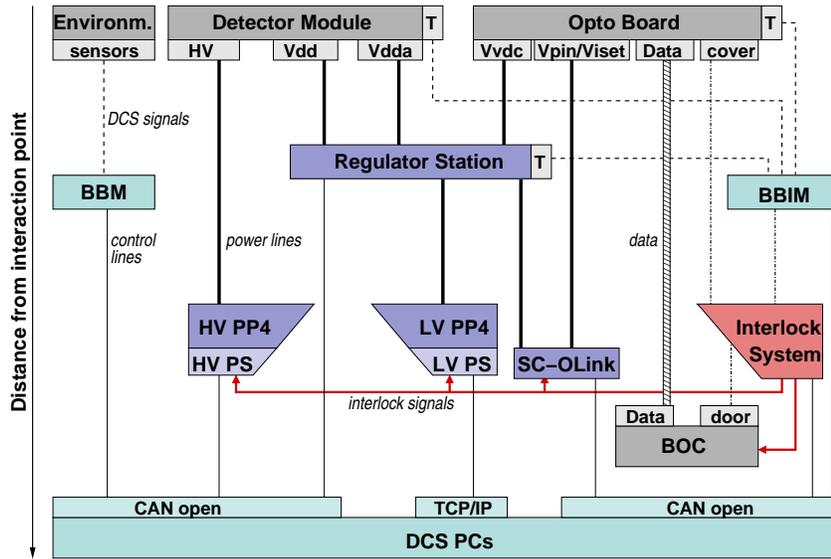


Figure 16: Overview on the hardware of the pixel detector control system.

- temperature and humidity sensors plus monitoring devices for their readout;
- multi channel current measurement units;
- the Interlock System;
- the DCS computers to control the hardware.

To comply with the ATLAS grounding scheme, all power supplies and monitoring systems must be floating. Radiation damage during lifetime operation of sensor and on-detector electronics requires that all power supplies have adjustable voltage outputs. For operational safety, over-current protection and interlock input signals are available in all the power supplies. The pixel power supply system has five main components: low voltage power supply (LV-PS), high voltage power supply (HV-PS), Regulator Station, Supply and Control for the Opto Link (SC-OLink), and the opto-board heater power supplies. Two low voltages supply the analog (V_{dda}) and digital part (V_{dd}) of the front-end read out electronics. Both are delivered by the LV-PS, which is a commercial component – the PL512M from WIENER⁷⁾. To protect the sensitive front end electronics against transients, remotely-programmable Regulator Stations are installed as close as possible to the detector. These Regulator Stations allow an individual tuning of the power lines through digital trimmers.

The pixel sensors are depleted by the high voltage V_{det} (up to 700 V) by the HV-PS. The HV-PS is assembled with EHQ-F607n_405-F modules provided by Iseg⁸⁾. The LV-PS and HV-PS are respectively connected to the low voltage patch-panel-4 (LV-PP4) and to the high voltage patch-panel-4 (HV-PP4) that are used to distribute the power and monitor the currents of the individual lines.

The SC-OLink, a complex channel consisting of three voltage sources and a control signal, delivers adequate levels for the operation of the on-detector part of the optical link. Monitoring of temperatures and of humidity is performed by the Building Block Monitoring (BBM) and the Building Block Interlock and Monitoring (BBIM) crates. While the first just provides a reading of values, the second additionally

⁷⁾WIENER, Plein & Baus GmbH, Burscheid, Germany

⁸⁾iseg Spezialelektronik GmbH, Rossendorf, Germany

creates logical signals, which are fed into the Interlock System. All components of the LV-PS, HV-PS, SC-OLink in addition to the BOC boards are connected to the hardware based Interlock System, that acts as a completely independent system. It consists of several units that guarantee safety for human operators as well as for detector parts. The Interlock System has high modularity; more than a thousand individual interlock signals are distributed. This high modularity has been chosen to keep low the number of detector modules out-of-service in case of some component failure. The Regulator System and parts of the Interlock System, installed inside the ATLAS detector, had to pass requirements of radiation tolerance; this required extensive qualification of many components.

Besides the LV-PS and HV-PS all other components in the system are custom designs, adapted to the pixel specific needs and using the Embedded Local Monitoring Board (ELMB) [36] for the monitoring through the DCS. ELMB is the ATLAS standard front end I/O unit for the slow control signal. The Control Area Network (CAN) interface of the ELMB and its CAN-open protocol ensure a reliable and robust communication. Different Openness, Productivity, Collaboration (OPC) servers are used to integrate the hardware into the higher level of the software. All together 630 CAN nodes on 43 CAN busses and 48 TCP/IP nodes for the LV power supplies are building the pixel control network. In total more than 44000 variables need to be monitored.

4.6.2 The Software of the DCS

The DCS software has to establish the communication to the hardware, to support the operator with all required monitoring and control tools, and to provide automatic procedures for safety and for easier operation of the detector for non DCS experts. Permanent operation and reliable data taking must be ensured. Additionally, operation of the detector requires good coordination of DAQ and DCS actions, and for the offline analysis relevant data must be recorded and stored into the conditions database. The core of the DCS software are the Prozess- Visualisierungs- und SteuerungsSoftware (PVSS),⁹⁾ projects, which run as a distributed system on eight control stations. As each part of a distributed system has its own control and data managers (processes inside PVSS), an independent development and operation of the different projects is possible. The core of the control software is the Front-end Integration Tools (FIT) which establish the communication with the hardware components. For each hardware component, like the HV-PS, the LV-PS and the different devices using the ELMBs, dedicated FIT exist. Each FIT consists of an integration and a control part. The integration part initialises each given hardware component and creates the data structures required to control it. The control part of the FIT instead supervises the operation of the same component. The hardware is mapped into the software in a device oriented way. The FITs are mainly foreseen for the DCS expert who needs to check the correct behaviour of the hardware. For persons that will run shift in ATLAS, a detector oriented view of the hardware is provided by the System Integration Tool (SIT). The mapping of the read-out channels to the detector devices is done by the SIT. The SIT creates a virtual image of the detector inside the DCS. It combines all information which is relevant for the operation of a detector unit like a half stave, a disk or the full detector. Furthermore the SIT is responsible for the storing of the data into the conditions database.

The software used to operate on the detector is the Finite State Machine (FSM), this software is developed in common from the four largest LHC experiments [37]. The FSM uses the geographical organised data structures, created by the SIT, and provides the user with a set of commands, to act on small or large fractions of the detector simultaneously. The actual status of the detector is returned by the FSM. Further, the proper settings and special power on sequences are performed automatically by the FSM. In addition, the FSM builds the link into the ATLAS wide control system. As part of the overall ATLAS control system, the pixel FSM will receive commands from the ATLAS FSM during normal data taking. The communication between DAQ and DCS is provided by DAQ-DCS Communication (DDC),

⁹⁾PVSS is made by ETM, Eisenstadt, Austria

which provides command transfer from the DAQ system to DCS, publishes DCS values to DAQ and vice versa. For the tuning of the optical link, the DDC is critical.

The DCS hardware and software system has been fully exercised in various configurations during the prototyping and construction phase of the pixel detector, namely in the test beams, with cosmic ray tests and during the integration of the pixel detector at CERN [38, 39].

5 Sensors

Sensors are the sensitive part of the pixel detector for charged particle detection and function as a solid-state ionization chamber. The sensor has to meet exacting geometrical constraints concerning its thickness and granularity as well as a high charge collection efficiency within the sensitive volume, while sustaining a massive amount of ionizing and non-ionizing particle radiation damage. This is reflected on one hand in the selection of the bulk material and on the other hand with the design of the pixel structure itself.

5.1 Design

The ATLAS pixel sensor is an array of bipolar diodes on a high resistivity bulk close to intrinsic charge concentration made by implanting high positive (p^+) and negative (n^+) dose regions on each on a side of a wafer. An asymmetric depletion region on the p^+ - n junction operates in reverse bias and extends over the whole sensor bulk volume, able to collect and detect all charges produced in the volume by ionizing particles. The sensor concept guarantees single pixel isolation, minimizes leakage current and makes the sensor testable as well as tolerant to radiation damage.

The pixel sensor consists of $250\ \mu\text{m}$ thick n -bulk with n^+ implants of size $400 \times 50\ \mu\text{m}^2$ on the read-out side¹⁰⁾ and the p - n junction on the back side. Aside from increased leakage current, radiation damage will invert the sensor bulk and then gradually increase the depletion voltage. For unirradiated sensors the depletion starts at the back (p) side and the pixels are not isolated from each other until full depletion of the bulk. Irradiation of the bulk leads to a change of the effective doping concentration N_{eff} : first N_{eff} drops and then runs through type inversion with increasing N_{eff} afterwards [40]. At the point of type inversion, the junction moves to the front (n) side isolating the pixels and enabling operation even if the bulk cannot be fully depleted. Maximum achievable depletion is still desirable to maximize the signal. The advantage of the depletion zone for the n^+ -in- n design is shown in Figure 17.

Oxygen impurities in the bulk ensure high tolerance of the silicon against bulk damage caused by charged hadrons [41, 42]. A comparison of the evolution of charge densities in standard and oxygenated silicon during irradiation with hadrons is shown in Figure 18a. In addition to the continuous irradiation of the sensors affecting the induced doping concentration, N_{eff} also evolves due to thermal effects. On short time scales, N_{eff} drops (beneficial annealing), runs then through a minimum of constant damage and finally on longer time scales increases again, (reverse annealing). See Figure 18b.

While the beneficial annealing is not altered in oxygenated silicon, both the constant radiation damage (N_C) is reduced and the reverse annealing (N_Y , see Figure 18b) is significantly slowed down [41, 42] producing a lower overall effective charge density in similarly irradiated samples after identical annealing scenarios. Sensors built from such material exhibit deeper depletion zones at the same bias voltage and full depletion at a lower bias voltage.

¹⁰⁾Per sensor tile 47232 pixel implantations are arranged in 144 columns and 328 rows. In 128 columns (41984 or 88.9 %) pixels have a size of $400 \times 50\ \mu\text{m}^2$ and in 16 columns (5248 or 11.1 %) pixels have a size of $600 \times 50\ \mu\text{m}^2$. In each column 8 pairs of pixel implantations near the center lines are ganged to a common read-out, resulting in 320 independent read-out rows or 46080 pixel read-out channels. This arrangement was chosen to allow the connection of the sensor tile to 16 electronic front-end chips, see section ??.

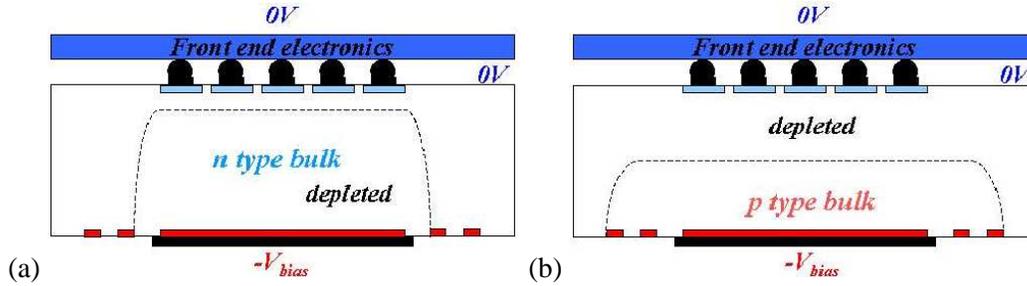


Figure 17: Comparison of depletion zones in n^+ -in- n pixel sensors before (a) and after (b) type inversion. Before type inversion the electrical field grows from the backside and reaches the pixel implants (full depletion). After type inversion the depletion zone grows from the pixel side and allows operation even if the bulk is not fully depleted.

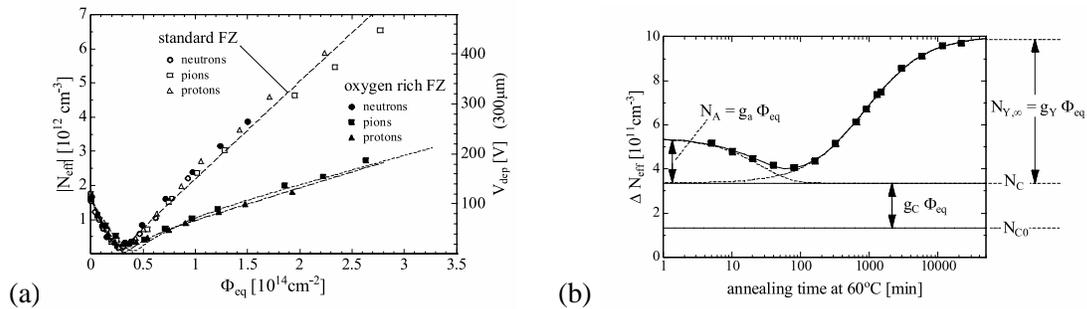


Figure 18: (a) Evolution of effective charge densities and full depletion voltage in standard and oxygenated silicon during irradiation with various hadrons. In oxygenated silicon the increase after type inversion induced by charged particles (pions, protons) is significantly lower. (b) Evolution of the effective doping concentration due to annealing and reverse annealing effects. The parameterization of this evolution is the so-called “Hamburg model” and represents an important input to the ATLAS pixel sensors which will operate near the point of minimal depletion voltages. In oxygenated silicon, both N_C and N_Y are reduced [41, 42].

By choosing an appropriate temperature profile (i.e. operation at 0°C, short periods of +20°C during detector access, cooling down to some –20°C during longer operation breaks of the experiment) one tries to keep sensors near the lowest possible N_{eff} and avoid reverse annealing to benefit from the lowest possible depletion voltage. Model calculations (Figure 19) of the combined effects of bulk irradiation and annealing have been performed [43]. The radiation induced increase of the intrinsic charge carrier concentration leads to higher leakage currents and contributes to noise also. Here, cooling of the sensors to values well below room temperature helps to reduce these effects.

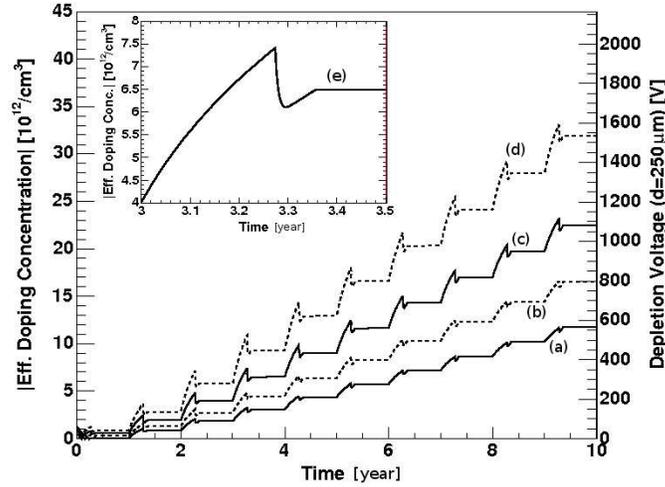


Figure 19: Change of the effective doping concentration (left scale) and the voltage necessary for full depletion (right scale) of oxygenated sensors according to irradiation and annealing effects under the Hamburg model for the two inner pixel detector layers in a standard (solid) and elevated (dashed) radiation scenario. (a) Layer 1 at 8.85 cm radial distance from interaction point with a standard fluence of $0.9 \times 10^{14} \text{ cm}^{-2} \text{ year}^{-1}$ (from the 3rd year of operation), (b) the same as (a) with a 50 % elevated fluence, (c) b-layer at 5.05 cm radial distance from the interaction point with a standard fluence of $2.4 \times 10^{14} \text{ cm}^{-2} \text{ year}^{-1}$, (d) the same as (c) with a 50 % elevated fluence. The enlarged detail (e) shows the evolution of the sensor characteristics during one year of assumed detector operation: 100 days of beam operation with irradiation at an operation temperature of 0°C, a period of about 30 days at +20°C during detector access, and cooling down to –20°C during the rest of the year.

The positive and the negative implanted sensor wafer sides are both structured by mask processes for implantation, metallization and deposition of silicon oxide and nitride. This double sided processing demands precise mask steps and incorporates front-to-back mask alignment on the order of a few micrometers. However, this allows for a segmented n^+ implantation used for definition of pixel cells and a guard ring structure on the p^+ implanted wafer side, locating the main voltage drop on the sensor surface opposite to the bump connections [44,45]. The 250 μm thick high resistivity silicon bulk of 2 to 3 $\text{k}\Omega/\text{cm}$ can be easily fully depleted before type inversion with bias voltages below 100 V. After type inversion the depletion zone grows primarily from the segmented n^+ implantation as the region of highest electric field into the bulk now converted to p-type.

On the sensor front side, pixel structures are arranged and isolated by moderated p-spray [45, 46] implantations which have been proven to be radiation tolerant with respect to surface damages induced by ionising charged particles for doses up to 50 Mrad in silicon. The principal layout is shown in Figure 20a. The dose of implant ions leading to the moderated p-spray isolation is regulated with a help of

a nitride layer which is opened during an additional mask step, creating a deeper high dose p-spray region in the center of the inter pixel gap and a shallower low dose layer everywhere else. This isolation technique avoids high field regions in the interface between pixel, isolation and bulk and ensures the radiation tolerance of the design [47, 48]

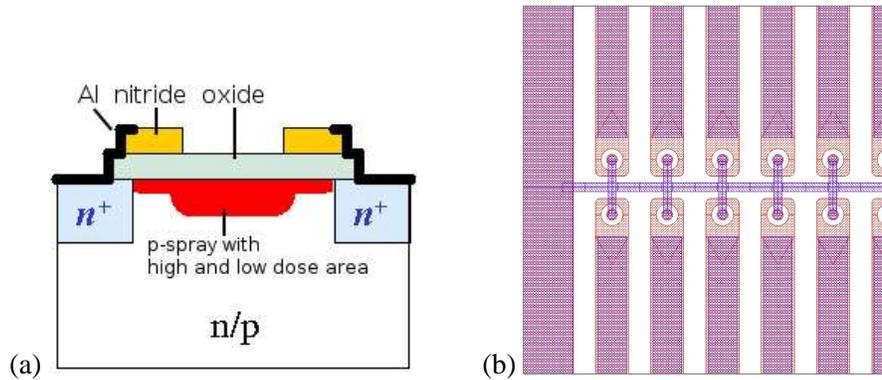


Figure 20: (a) Principal layout of the moderated p-spray isolation which consist of high and low dose areas between the n^+ pixel implantations in the n bulk. Compared to other isolation profiles like p-stop [49] and p-spray [46] high field regions are avoided in the transition regions between pixel and bulk. (b) Layout detail of the bias grid [45] visible in the production mask for a pixel double row.

All 46080 read-out channels of an entire sensor tile are connected to a common bias grid structure [45] (Figure 20b) employing a punch-through connection technique to each channel which biases the whole sensor without individual connections, but still ensures isolation between pixels. This bias grid has been used for quality assurance measurements before any read-out electronics is connected to the sensors. An opening for each pixel in the passivation layer of the sensor allows a connection to each channel using a bump-bond technique (see section ??) to front-end electronics (see section ??), which is DC coupled and provides biasing for each individual pixel.

5.2 Prototyping and tests

Bulk and surface design features of the sensors have been extensively tested during the prototyping [48] and a dedicated pixel sensor quality assurance plan was developed [50]. The sensor layout has been designed on four inch diameter double-sided wafers, which include three sensor tiles of about $18\text{ mm} \times 62\text{ mm}$ each. During the prototyping, dedicated test structures were developed. The test structures were placed on the ATLAS pixel sensor wafer surrounding the sensor tiles to allow dedicated electrical tests of various design features of the sensor (Figure 21).

The quality control included mechanical as well as electrical inspections and tests. Examples of visual and mechanics tests are unique wafer identification with the help of scratched serial numbers, visual inspection of the surface quality, a check of the mask alignments, planarity as well as thickness measurements of wafers. Electrical tests included measurement of the leakage current and the capacitance of diodes with the guard ring structure. Leakage currents were monitored on sensor tiles, and on test structures. Current and capacitance measurements were performed on oxide structures.

As an example of the bulk characteristics, the dark current on sensor tiles is monitored. The break down voltage is required to be well above 150 V. Figure 22 shows an example of measurements performed during the prototyping. While the two blue curves are examples of practically perfect diodes,

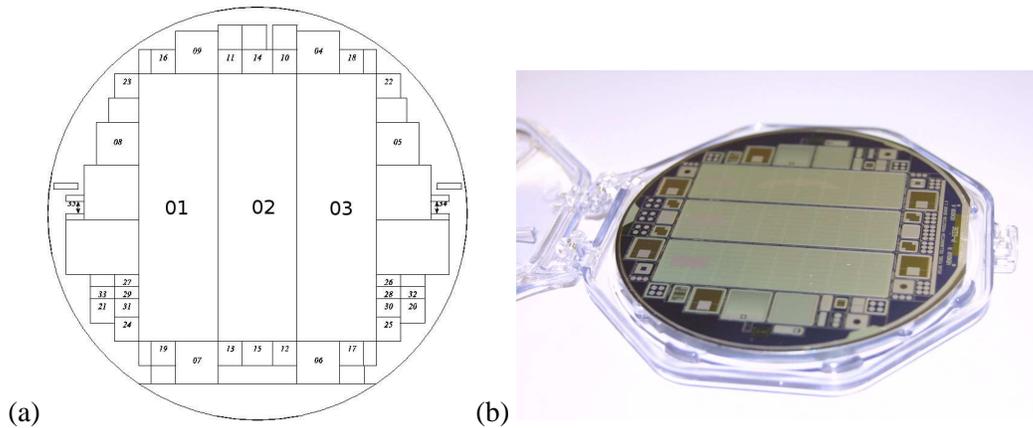


Figure 21: (a) Geometrical layout of the sensor wafer. Central large structures 01, 02 and 03 are the sensor tiles carrying 46080 read-out channels employed in the ATLAS pixel sensor modules; structures 04 to 35 are dedicated test structures to monitor the quality of prototyping and production. (b) A pictorial view of the 4 inch diameter ATLAS pixel sensor wafer (p-side view).

the black curve shows a break down between 150 and 200 V and the red curve shows a very steep break down behaviour near the typical depletion voltage indicating a defect on the n-side of the sensor.

Since the moderated p-spray dose is one of the critical issues for the sensor design, the measurement of the p-spray dose is an important quality control test. Here, dedicated punch-through structure as well as an oxide structure is needed to determine the oxide capacitance. An example of a punch through measurement is shown in Figure 23. The idea of this measurement is to determine the current I between an individual pixel and the bias grid (Figure 23a) as a function of the potential difference ΔV while the sensor bulk is biased at -150 V. The resulting current (Figure 23b) increases for good isolations at $\Delta V > 1$ V. This together with the oxide measurement (not shown here) leads to the p-spray dose [50]. This example shows the necessity for advanced quality control measurements to assure the radiation hardness of production sensors. A few sensors had to be rejected due to these criteria during the production process.

One important aspect of the present ATLAS pixel sensor is the operation under irradiation, especially near the end of its lifetime. Here, the main limitation of the sensor is the trapping of charge carriers in the silicon bulk which leads to a decreasing value for the collected charge during the operation time of the detector. Trapping times have been determined in test beam [51], and lab set-ups [52]. Based on the operation model (cf. Figure 19) of the ATLAS pixel sensor, the expected collected charge for minimum ionizing particles passing through the $250 \mu\text{m}$ thick bulk has been predicted to be between 15 and 19 ke after irradiation fluxes of 8 to $12 \times 10^{14} \text{ cm}^{-2}$ [53]. These are expected after 10 years of operations for sensors in layer 1 of the ATLAS pixel detector. Values agree nicely with those derived from test beam results performed using production-like sensors [54]. Further performance features, including those of the sensor, were extracted under test beam conditions, which are summarized in section ??.

5.3 Production and quality assurance

Sensor tiles have been produced by two independent vendors, who went through the prototyping and qualification process. Based on the experience during prototyping, specialized quality assurance procedures were employed for the series production of sensors [55, 56] and were carried out as collaborative effort at four different pixel sensor institutes. Extensive cross calibration of mechanical and electrical

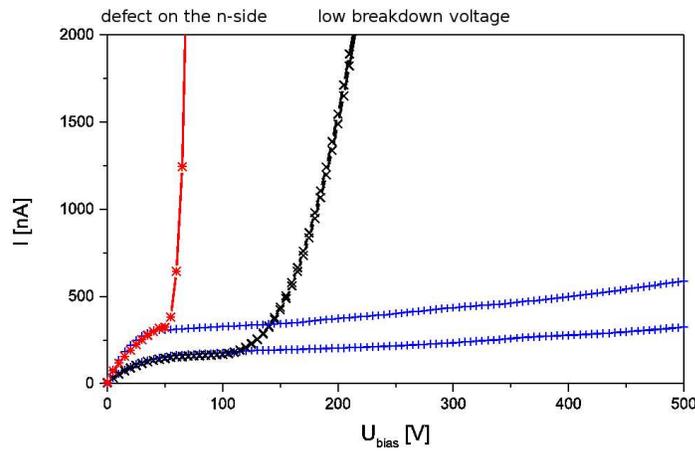


Figure 22: Examples of dark current vs. bias voltage curves on pre-series sensors tiles. While the two blue curves are examples of practically perfect diodes the black curve shows a break down between 150 and 200 V and the red curve shows a very steep break down behaviour near the typical depletion voltage indicated a defect on the n-side of the sensor.

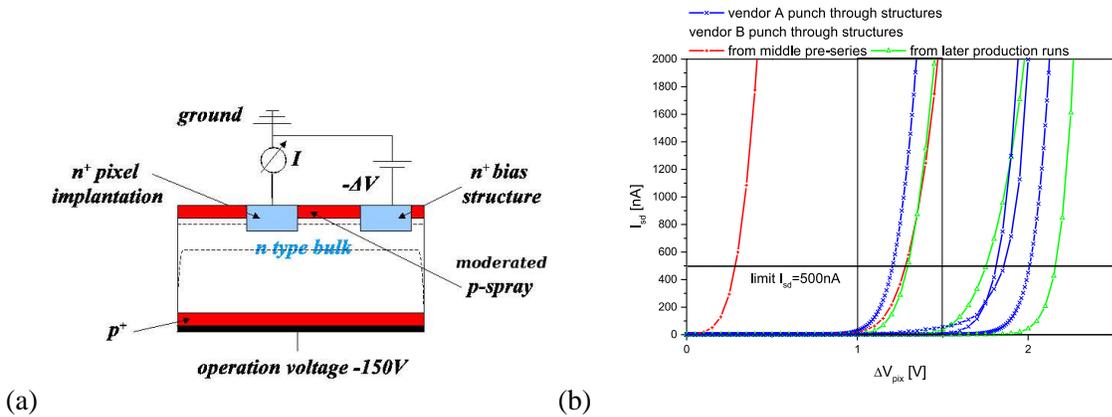


Figure 23: (a) Electrical set-up to monitor the bias dot current vs. the potential difference test on a depleted substrate. (b) Example of punch through current measurements on several prototype structures at the nominal bias voltage of 150 V. The left red curve is an example of a too low potential difference, which occurred during the early prototyping, compared to later productions, which fulfilled the isolation criteria of more than 1 V.

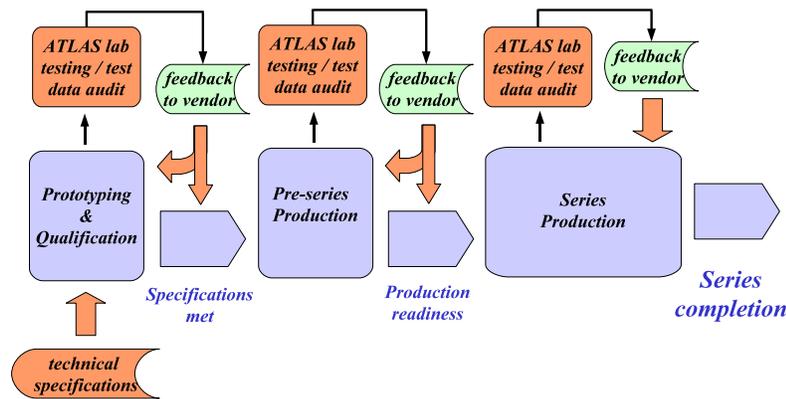


Figure 24: Information feedback for the sensor quality optimization during the various production steps of ATLAS pixel sensor wafers.

measurements was performed during these processes. The schematic layout of the information feedback between sensor institutes and vendors during the various production steps are sketched in Figure 24.

The rate of production of ATLAS pixel sensors is shown in Figure 25. More than 2200 sensors successfully passed through the quality assurance process and were available for hybridisation [57] to the front-end electronics.

6 Modules

6.1 Overview

The sensitive area of $\sim 1.7 \text{ m}^2$ of the ATLAS pixel detector is covered with 1744 identical modules, independent of their spatial position, with a small exception (see below). Each module has an active surface of $6.08 \times 1.64 \text{ cm}^2$. A module is assembled from the following assembly parts

- the sensor tile containing 47232 pixels covering an area of $6.34 \times 2.44 \text{ cm}^2$
- sixteen front end electronics chips (FE) each containing 2880 pixel cells with amplifying circuitry, connected to the sensor by means of fine-pitch bump bonding (see section 6.2)
- a $50 \mu\text{m}$ thin, fine-pitch double-sided flex-kapton foil onto which routings for signal and service traces are done
- a module control chip (MCC) situated on the flex-kapton foil
- for the barrel modules another flex-kapton foil, called a pigtail, provides the electrical connection to the outside through a connector to which a micro cable is attached; for the disk modules the micro cables are attached without the pigtail connection (see section ?? for a description of the microcables).

The concept of the ATLAS hybrid pixel module is illustrated in Fig. 26. Sixteen front-end chips are connected to the sensor by means of bumping and flip-chip technology. Each chip covers an area of $0.74 \times 1.09 \text{ cm}^2$ and has been thinned before the flip-chip process to $\approx 190 \mu\text{m}$ thickness by back-side grinding. A sizeable ($\approx 25\%$) fraction of the front-end chip is dedicated to the End of Column (EoC) logic. Once bonded, most of the EoC logic extends out of the sensor area. Wire bonding pads at the

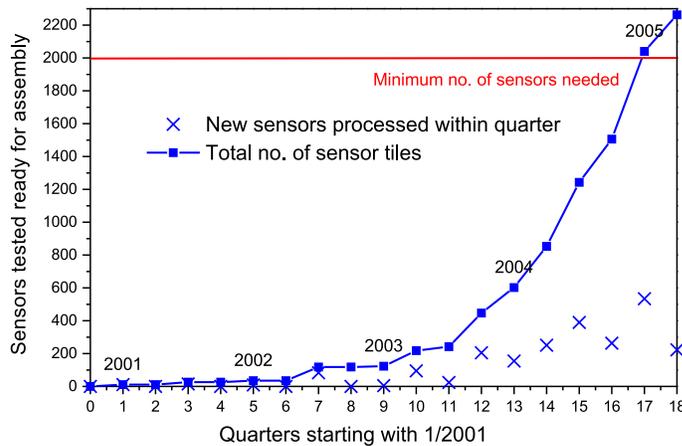


Figure 25: Sensor tile output in sum and per quarter for the ATLAS pixel laboratories in total during the production process.

output of the EoC logic are thus accessible to connect each front-end chip to the μ ex-hybrid kapton foil by means of Al wire wedge bonding. On the μ ex-kapton foil, copper traces route the signals to the Module Control Chip (MCC). The MCC receives and transmits digital data out of the modules. The μ ex-kapton circuitry is also used to distribute properly decoupled low voltage to all chips. These lines are dimensioned such that the voltage drop dispersion on the μ ex be limited to ≈ 50 mV in order to keep all chips in the same operating range. The substrate material must have a low pin-hole probability, as it also houses high voltage (≈ 600 V) traces for the sensor bias. The kapton material must not degrade after the LHC (500 kGy) irradiation doses. Passive components are added to the μ ex-hybrid kapton for decoupling and filtering of the front-end chips.

The module temperature is remotely monitored via a Negative Temperature Coefficient (NTC) resistor placed on the kapton circuit, and a fast interlock powers off a module when overheating occurs. The interlock is necessary as the large power density and the low mass of the support and cooling structure imply temperature rises of up to 10 degrees per second in case of a cooling fault.

A complete module draws 1.2 A at 1.6 V on the analog supply and 0.8 A at 2 V on the digital supply, i.e about 3.5 W per module. This value is expected to increase to about 5 W after an accumulated dose of 500 kGy.

The bump and flip-chip operation results in a so-called bare module. The sixteen chips of an assembled module are first tested on a probe station to detect defects and possibly rework the module which can only be done at this point of the assembly chain.

Region in between Chips

The sensor pixels have dimensions of $50 \mu\text{m} \times 400 \mu\text{m}$, except for 11% which have a size of $50 \mu\text{m} \times 600 \mu\text{m}$, to allow for a contiguous sensitive area between chip boundaries in the long pixel direction. In the perpendicular direction, two times four pixels under each of the two adjacent chips cannot be covered by active pixel circuitry. These off-side sensor pixels are connected through metal lines on the sensor to 4 + 4 neighboring electronics pixels at the top of the columns in addition to the cells which lie directly underneath as is illustrated in Fig. 27. The resulting hit ambiguity is resolved by off-line pattern recog-

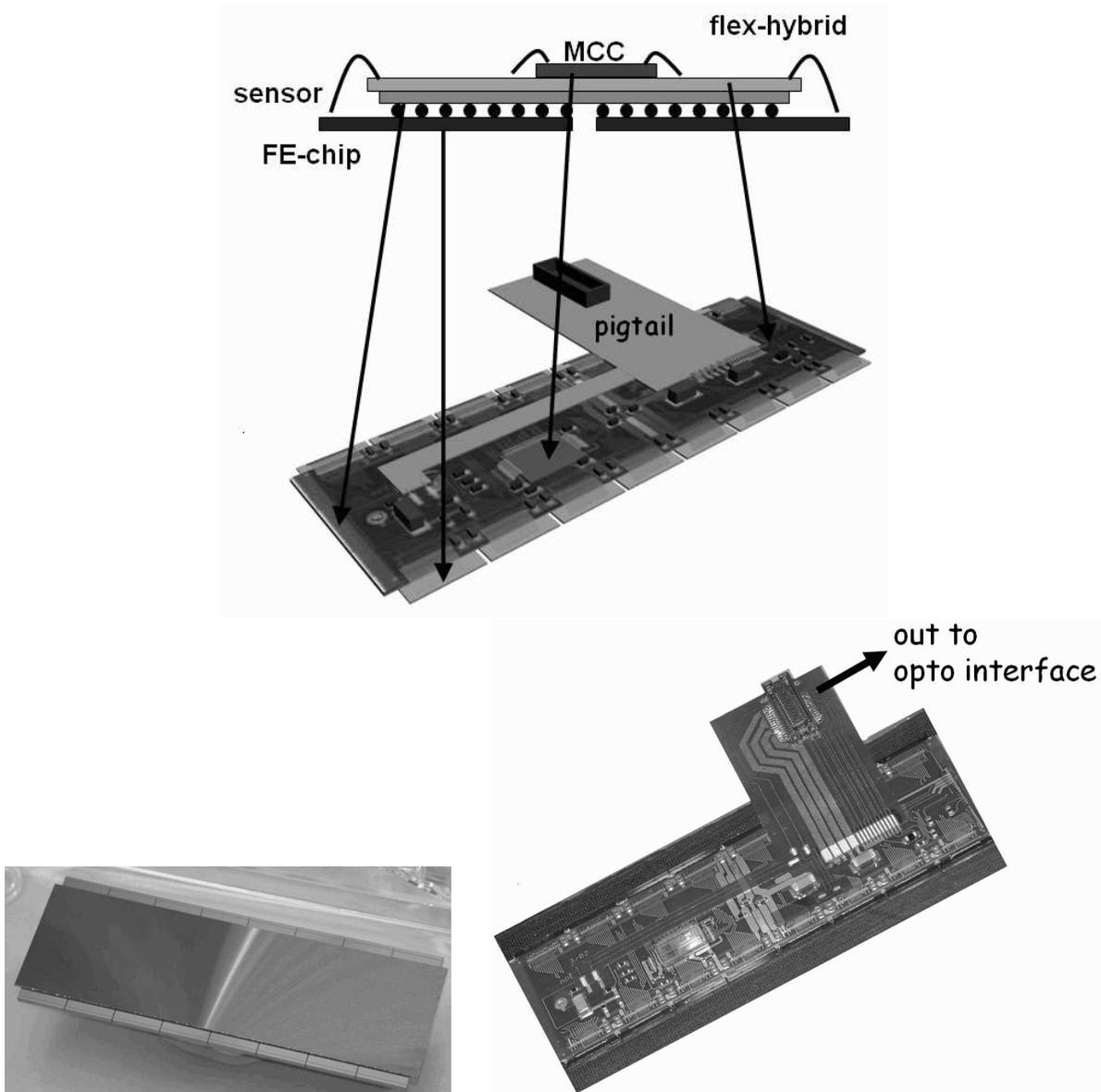


Figure 26: The barrel pixel module. (top) overview, showing the components of the module assembly: sensor, FE-chips, Flex-kapton-hybrid, module control chip (MCC), pigtail. (b) photograph of a bare module, (c) photograph of a fully assembled module.

inition software. These special pixels: the $600\ \mu\text{m}$ size (long pixels), the pairs connected to a single readout channel (ganged pixels) and the ones below the metal line connecting two ganged cells (inter-ganged pixels) have slightly degraded electrical performances due to the increased sensor capacitance (see section 6.6).

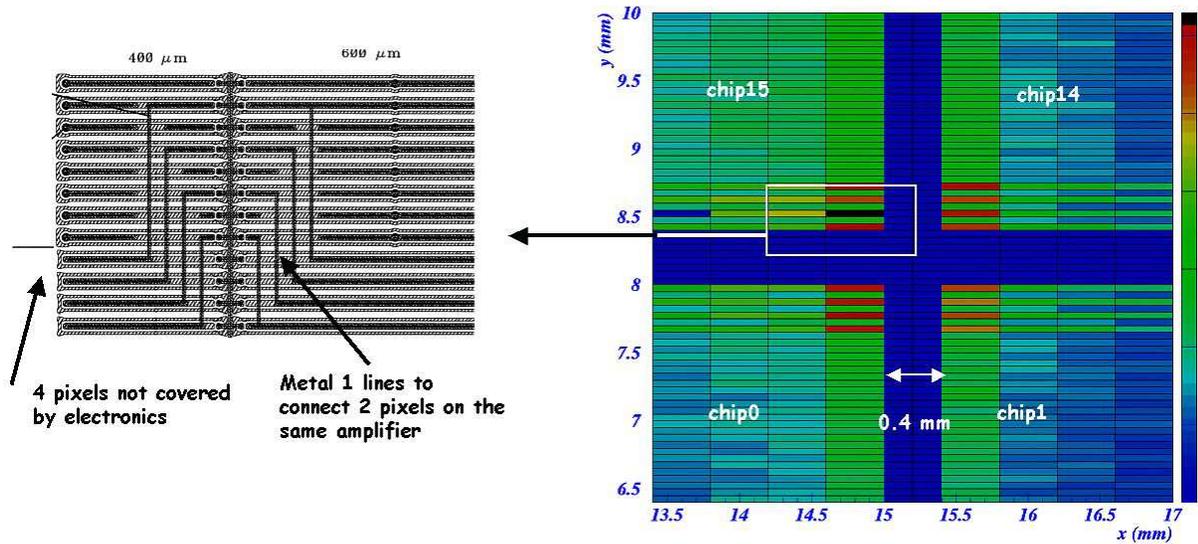


Figure 27: End region of the pixel detector at the edge of four FE-chips. The area of the sensor covered by the chip edges is marked in grey. The pixels in between the chips (white rectangles) are connected through metal lines to another pixel underneath the chips.

6.2 Bump Bonding

Bump bonding is extensively used in the electronics industry for the attachment of integrated circuit dies to printed circuit boards or other substrates. Two different bump bonding techniques have been used for ATLAS: electroplated solder (PbSn) bumping [58, 60] and evaporative indium bumping [61]. Both bump deposition processes are done at the wafer level. The principle of a bumped sensor – electronics pixel element is sketched in Figure 28. The substantial demands on the handling require that the wafers get bumped with their original thickness ($\sim 700\mu\text{m}$ for the 20 cm IC wafers). Wafer thinning is done after bump deposition by covering the bumps with a photo resist layer and a UV releasing tape for bump protection and for handling. The wafers are then thinned by backside grinding to $180\mu\text{m}$ – $190\mu\text{m}$. They are diced and singulated immediately afterwards and then they are tested again on a probe station to assure that they are still functional and ready for the π ip-chip process.

6.2.1 The Solder Bumping and Bonding Process

In eutectic PbSn solder bumping [58, 60], the solder is deposited through electroplating. On an “under bump metallization” (UBM), which is a set of several metal layers sputtered on the contact pad for reasons of adhesion, diffusion barriers and wettability, a *PbSn* cylinder is galvanically grown and melted to a sphere on the chip wafer, while the sensor wafer receives only the UBM [59, 62]. The parts are mated by π ip-chipping with re π ow which provides self-alignment. The process π ow is displayed in [65]. The distance between chip and sensor is about 20 – 25 μm , thus minimizing the cross-talk between electronics and sensor. The connection resistance is smaller than 1Ω and the ultimate shear stress is $\approx 50\text{MPa}$. Pictures of a small dimension *PbSn* bump after re π ow and of a sequence of bumps on an ATLAS FE-chip are shown in Fig. 29.

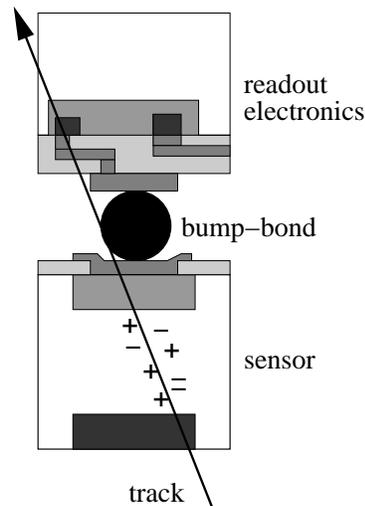


Figure 28: Blow-up sketch (not to scale) of the cross section of a hybrid pixel detector, showing one connection between a sensor and an electronics pixel cell. A particle track releases ionization in the sensor volume

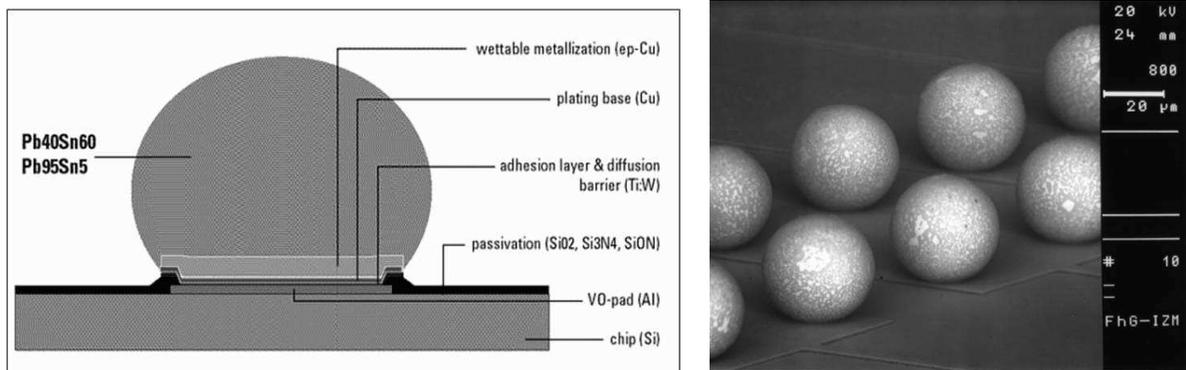


Figure 29: left) Built-up of a eutectic PbSn solder bump [58, 60], (right) rows of a PbSn bumps (courtesy IZM-Berlin).

6.2.2 The Indium Bump Bonding Process

In the case of indium bonding, the bumps are grown by deposition of evaporated indium on both mating parts [63]. Bump pitches can be as low as $30\ \mu\text{m}$, but the bump height is limited to $10\ \mu\text{m}$ due to the use of a lift-off process for the removal of the polyimide evaporation mask. Bumps are deposited both on the sensor and on the electronics. Mating is obtained by *In-In* thermocompression. The process flow is shown in [65]. Figure 30 shows a micrograph of $50\ \mu\text{m}$ pitch Indium bumps deposited on two glass samples and then chip chipped together [61] at a temperature of $\sim 100^\circ\text{C}$ applying a pressure of about $20\ \text{N}/\text{cm}^2$ per chip. The distance between chip and sensor after bonding is $\approx 10\ \mu\text{m}$.

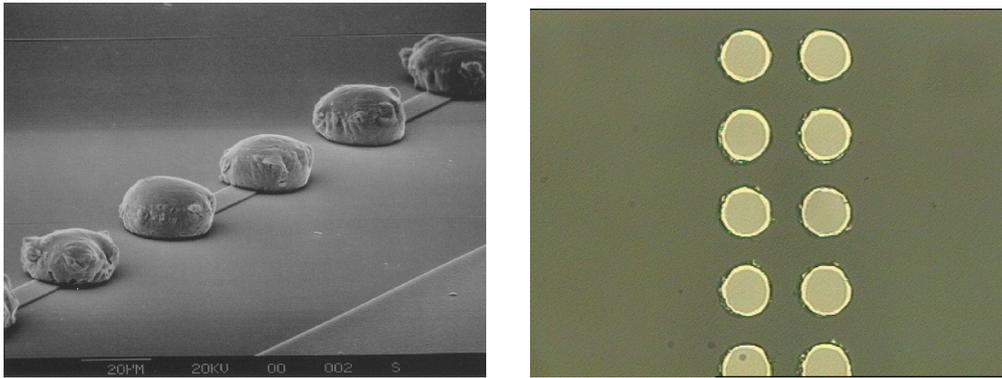


Figure 30: Micrograph of a Indium bump deposition on Silicon at $50\ \mu\text{m}$ pitch (left) and of a π ip-chip assembly of two $50\ \mu\text{m}$ pitch bump arrays (right) on glass substrates (courtesy SELEX Sistemi Integrati, Rome) [61]

6.3 Quality Control of Bump Bonded Assemblies

Inspections before and after π ip-chip assembly are crucial to obtain the highest yield for functional pixel modules. Automated inspection of bumped wafers with the combined use of a television camera and laser interferometry allows to find missing bumps, merged bumps, deformed bumps or other defects as well as to measure bump height on wafers. Inspection with high resolution ($2\ \mu\text{m}$) X-ray machines allows one to detect misalignment or merged/bridged bumps previously not detected or caused by the π ip-chip process. Both solder and indium bump bonding have been used to produce more than 2000 pixel modules by two different firms with bump defect rates of $\approx 10^{-5}$ – 10^{-4} at wafer level and $\approx 10^{-4}$ – 10^{-3} after π ip-chip.

6.4 Reworking of Bump Bonded Assemblies

All modules were built with Known Good Die (KGD), i.e. all die are tested prior to π ip-chip and only the good ones are used. This is a crucial requirement as the module yield goes with the n^{th} power of the electronics chip yield, n being the number of chips per module.

All front-end chips are also electrically tested after bump bonding, in order to check damages of the front-end electronics or bumps for which the quality electrical contact is not adequate.

Both solder and indium bump bonded modules have been successfully reworked [62, 64] with a success probability of more than 95%. In both cases the operation requires heating and application of a force pulling off the die to remove it, while leaving some metal on the bond pads. Afterwards, a new die is π ipped to the sensor. The probability to properly connect all pixels in the second π ipping is very high.

6.5 Module assembly

Once a bare module has passed the acceptance test, it is equipped with a π ex hybrid to provide the connections between the Module Controller Chip and the front-end electronics and from the Module Controller Chip to a microcable. A photograph is shown in Figure 31.

The π ex hybrid is a double sided π ex printed circuit with $50\ \mu\text{m}$ substrate thickness and $25\ \mu\text{m}$ Cu lines, manufactured by Dyconex AG (Bassersdorf, CH). It has been specifically designed to cope with the maximum 600 V depletion voltage applied to the sensor. Besides the above mentioned connections, it includes also passive components for local decoupling and an NTC for monitoring of the module temperature.

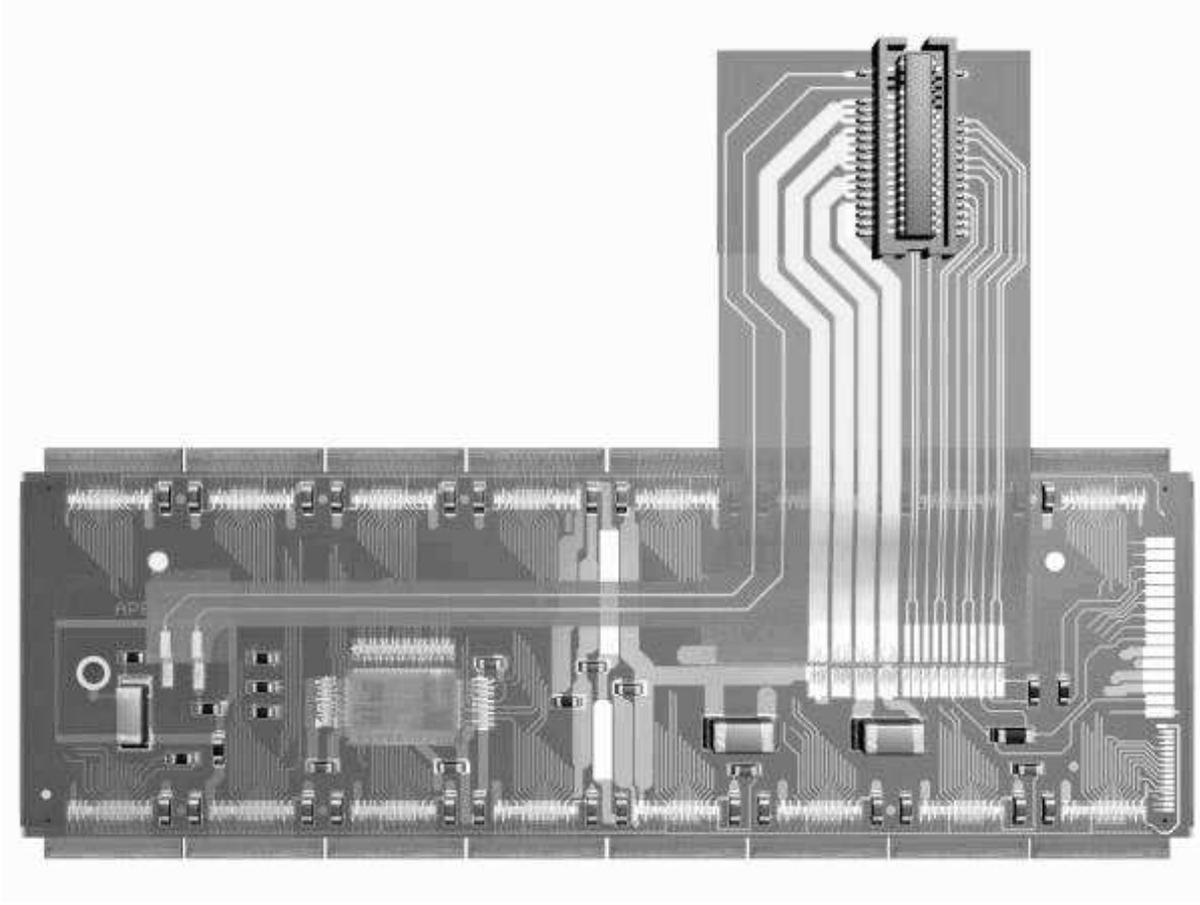


Figure 31: Picture of an ATLAS Pixel barrel module

To facilitate testing of μ ex hybrids, they are laminated on custom made printed circuit boards (Flex Support Card or FSC), which were used for handling of the μ ex themselves and after module attachment. A module is cut out from the FSC just prior to loading on the local support (see section ??).

Flex hybrids for barrel and disk modules are identical. A difference appears only when the connector for the link to the services is attached. For barrel modules, an additional μ ex circuit (pigtail) is glued on top of the μ ex hybrid and electrically connected by wire bonding. It has a zero-insertion-force connector which is fixed to the back side of the stave and used for attachment of the low-mass type-0 microcables (see section ??). Disk modules instead use higher mass copper cables that are soldered directly on the μ ex hybrid.

Because of the very different coefficient of thermal expansion, between kapton and silicon, the glue used for attachment of the μ ex hybrid to the bare modules needs to be distributed in a way to avoid any excessive mechanical coupling between the two. On the other hand, a strong binding is required in the places where wire bonds are needed. Therefore, glue (Dow Corning SE4445) is deposited along the pads lines used for the interconnection between the μ ex hybrids and the front-ends, below the MCC, near the high voltage bonding pad and, for barrel modules, below the pigtail attachment point.

6.6 Testing and selection procedure

After loading on a FSC a module can be connected to a test setup using cables with similar characteristics to the ones that will connect the modules to the optoelectronics in ATLAS. The test setup in the laboratory

uses LVDS signals. The readout chain and control software is the same as that used for the FE and bare module testing, except now configured to communicate via the MCC and uses the microcable instead of probe needles for connection to the integrated circuits.

The characterization procedure [66, 67] aims to certify if a module is acceptable for operation in ATLAS, both from the electrical and mechanical points of view. A ranking value is determined such that better modules can be selected for the most critical parts of the detector. In particular a module must satisfy the following conditions:

- the electronics should be tunable and have enough operation range to guarantee there will be tuning capability to operate even after heavy radiation damage;
- the bump bonding has not been damaged by the assembly procedure and is sufficiently strong;
- the wire bonding of MCC and FE is done correctly and is sufficiently strong.

The testing sequence proceeds as follows:

1. a basic series of electronics tests is performed at room temperature after module assembly;
2. modules undergo a mechanical stress test, being cycled 10 times between room temperature and $-30\text{ }^{\circ}\text{C}$, with a cycle length of about 2h;
3. electronics tests at room temperature are repeated after thermal cycling and compared to the initial tests;
4. a complete module characterization is performed at $-10\text{ }^{\circ}\text{C}$, which is the expected operating temperature.

The last test is the most relevant for the definition of module quality and selection for usage in the detector. Reduced electronics test are also performed after loading of modules into the local supports, to monitor possible damage happening after loading, which may trigger the repair or replacement of a module.

Room temperature tests consists of

1. a basic functionality test: the module can be configured, the readout chain is tested by the digital injection and the amplifier cells operated by the analog injection;
2. a test of module tunability: thresholds are equalized to 4000 e;
3. a threshold scan without depletion voltage applied to the sensor.

The first test is mainly a check of correct wire bonding or electrostatic discharge damage to the electronics. In the second test pixels can usually be tuned to the target threshold with a dispersion of 60 e, and a noise which ranges between 120 e for standard pixels to 300 e for long and ganged pixels (Figure 32).

The second and third tests are also sensitive to bump bonding properties. Pixels which fail the tuning usually correspond to a cluster of merged bumps. In this case several cell amplifiers are shorted together, resulting in reduced sensitivity to the injected pulse. In the case of an undepleted sensor, instead, normal pixels are affected by the large parasitic capacitance of the sensor, but pixels not connected to the detector stand out because the noise level remains low, independently of the bias voltage applied to the sensor side. Example of modules with such defects are shown in Figure 33.

During the detector construction, the test of modules before and after the thermal cycles has been of paramount importance:

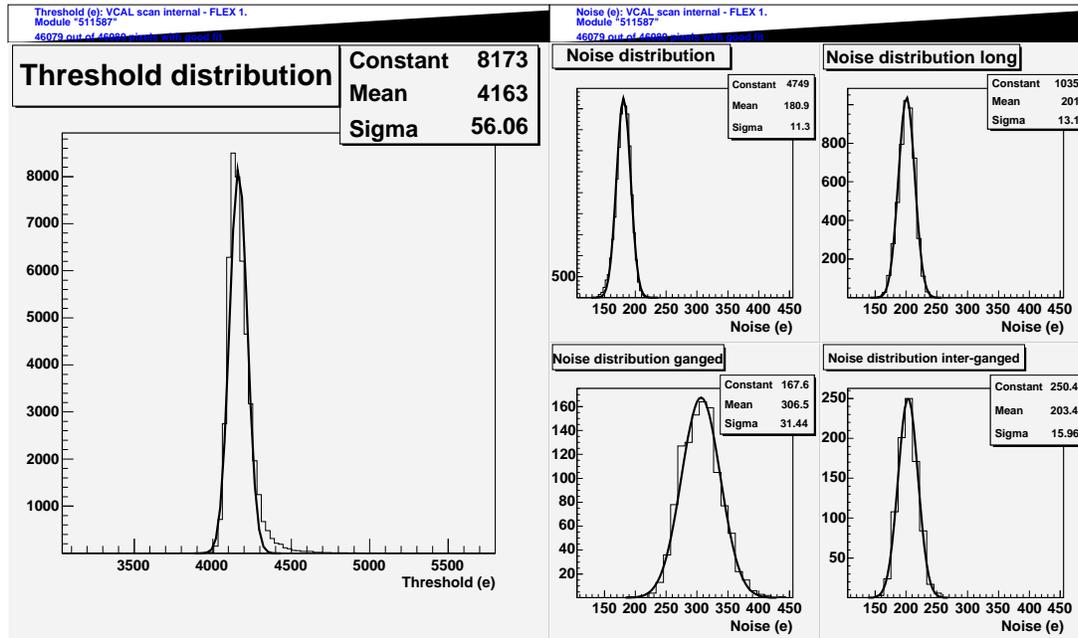


Figure 32: Threshold (left) and four noise (right) distributions - for different locations and types/sizes of pixels - of a typical module (normal, long, ganged, inner-ganged). The thresholds are uniform for the entire modules.

- debugging the failures observed in the functionality test, a problem in the potting technique for the MCC was found, which resulted in unreliability of the wire bonds, which has been corrected for the whole production;
- comparison of bump damage between the initial assembly and the end of thermal cycling, allowed to disentangle damages due to bad handling during the assembly, which are done once and are stable in time, and damages due to weak bonds, for which there is a steady increase of disconnected bumps with time.

The full characterization at the nominal operational temperature of $-10\text{ }^{\circ}\text{C}$ includes additional checks of tunability and operational range:

- MCC operation was checked between 1.6 and 2.5 V, showing a typical turn-on at 1.8 V.
- FE operation was tested within wide ranges of digital and analog low voltage supply (VDDA 1.5-2.0, VDDD 1.9-2.3).
- The amplifier feedback current was tuned so that the average ToT response to a minimum ionising particle corresponded to 30 clock cycles: with the LVL1 trigger latency expected during operation, this setting provided 99.5% efficiency in a test beam [68]
- Timing measurements have been performed to check the timewalk performance of the FE electronics when attached to the sensor. The overdrive needed to assign a signal to the correct beam crossing is about 1000 e.
- A measurement with the 60 keV X-ray of an ^{241}Am source, checked the detector's response to a signal delivered directly to the sensor (see Figure 33).

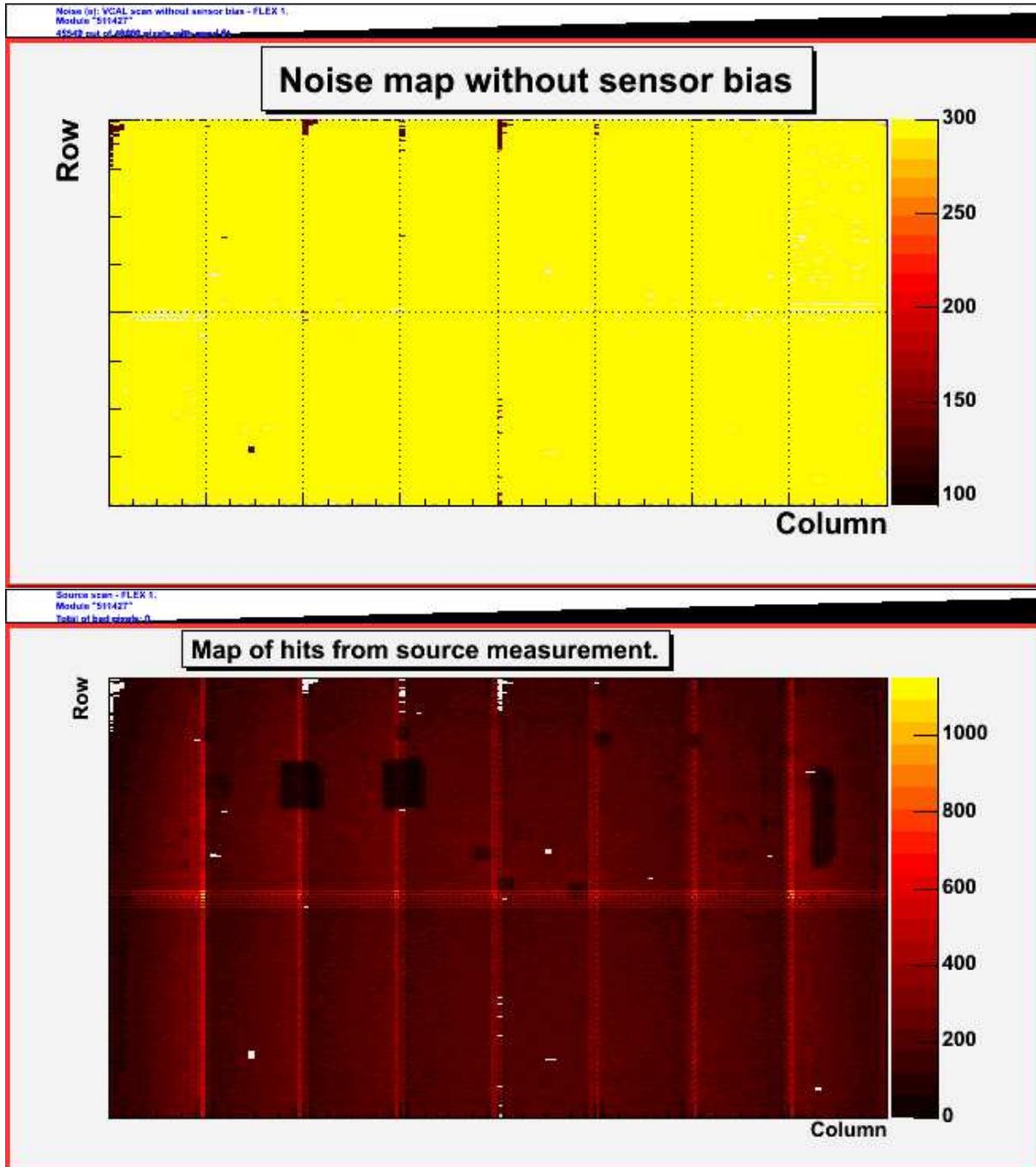


Figure 33: Noise distribution for a Selex module without sensor bias (top). Disconnected regions are visible as low noise spots. For comparison below is a hitmap obtained with an ^{241}Am source.

The source measurement is especially relevant in accessing module quality, since, being self-triggering, is very sensitive to noisy channels. The duration of the measurement is chosen to reach an expected occupancy of at least 10 hits in every pixel channels. Therefore it is also very effective in uncovering inefficient cells, due to merged or disconnected bonds.

The number of dead channels at the source test is the first entry in a ranking function which has been chosen in order to evaluate module quality. Besides defective channels this function includes:

- a χ^2 -like term, describing how the analog performance of a module differs from the average one;
- penalties for anomalous values of the leakage current or module bowing, which may give problems during operation;
- penalties for any repair operation performed on the modules.

This ranking function was used for module selection for further assembly. The distribution of the ranking function is displayed in Figure 34. The bump in the ranking distribution around 300 corresponds to the set of modules that needed a full rebonding of the MCC, because of the potting problem mentioned above. The B-Layer has been built using modules with penalty lower than 60, corresponding to a channel inefficiency better than 0.13%. Modules with penalties higher than 1000 were not accepted for assembly. Analysis of the ranking showed an overall equivalence of all the different assembly laboratories, while pointing out a clear difference between the two bump vendors.

The main reason for the difference is the higher number of disconnected bumps in the In-bumped modules. As stated before, a clusterized set of disconnected bumps may be the seed for a widening of the disconnected region. Because of that a ranking penalty of 202 was added for each FE chip containing more than 30 disconnected bumps. In hindsight this penalty has been found to be quite conservative, but it is the main reason for the tails in Figure 34.

During the final phase of module production, when it was clear that there were a sufficient number of spare bare modules, only the ones with clusters of less than 4 disconnected bumps were selected for module assembly, resulting in an improvement of module ranking.

6.7 Production yield

Statistics for the production yield of bare modules are summarized in Table 6. Most losses were due to sensor damage, bad bumping and FE damage.

Sensor damage usually is detected by an early breakdown voltage in the sensor tiles previously passing the sensor quality cuts. The lossrate was similar for both bump vendors and results in about 3% of the modules being rejected.

Bad bump bonding and FE damage were repairable according to the reworking procedures outlined previously. The failure rate and the possibility of reworking differed between the two bump vendors.

In the case of bump problems, IZM often performed internal reworking after the in-house X-ray inspection, reprocessing the bumps. For indium bumps, there was no possibility to reprocess the bump deposition. If the damage was too widespread, the module was not submitted for reworking. This resulted in an overall higher failure rate.

FE damage was due to silicon shards trapped between the sensor and the FE chip, which, during chip-chipping break the surface of the FE chips, resulting in shorts between the metal layers. The problem was much more severe on Indium-bumps, given the smaller bump height. Replacement of the FE chip usually resolved the problem, but manually removing the shards from the detector surface was needed to reach a good reworking efficiency. Statistics for the production yield of modules are summarized in Table 7.

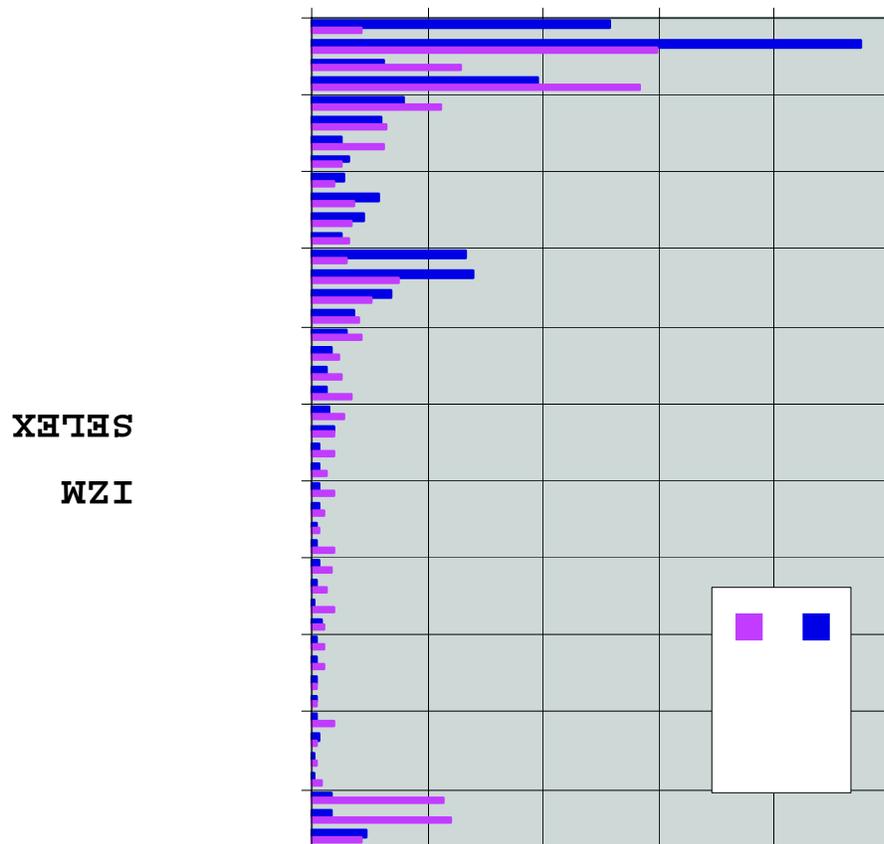


Figure 34: Module ranking distribution.

	Selex		IZM		Total	
	modules	yield	modules	yield	modules	yield
Assembled	1468		1157		2625	
Rejected	172	11.7%	35	3.0%	207	7.9%
Accepted	1296	88.3%	1122	97.0%	2418	92.1%
as delivered	1101	75.0%	1035	89.5%	2136	81.4%
after reworking	195	13.3%	87	7.5%	282	10.7%

Table 6: Bare modules production yield

	Selex		IZM		Total	
	Modules	Yield	Modules	Yield	Modules	Yield
Assembled	1190		1122		2312	
Accepted	1025	86.1%	1075	95.8%	2100	90.8%
B-Layer quality	281	23.6%	445	39.7%	726	31.4%
not B-layer quality	744	62.5%	630	56.1%	1374	59.4%
Not accepted	165	13.9%	47	4.2%	212	9.2%
Ranking ₁₀₀₀	68	5.7%	10	0.9%	78	3.4%
at least one dead FE	71	6.0%	10	0.9%	81	3.5%
could not complete testing	26	2.2%	27	2.4%	53	2.3%

Table 7: Module production yield

Modules which did not complete the testing were usually due to mechanical damage observed after the assembly procedure, either induced by handling or because of weak parts which had passed the previous quality control steps.

Modules containing one or more FE which could not be operated were also discarded from the production path. A loss of about 1% was due to defects in the path from the MCC to the FE through the α x hybrid. For Indium-bump modules, the additional yield loss is due to shorts on the FE, similar to the behavior observed on bare modules. These defects are concentrated on reworked modules and modules that underwent multiple shipments. They can be assumed to be the same defect of crystal shards as seen on bare modules, which is not present after the initial bonding, but is finally produced by the additional mechanical stress in the module assembly.

Besides these two classes, all the other modules were operational, and a ranking is used to select the best ones. The difference in ranking distribution between the Indium and solder bump modules is mainly due to regions of disconnected bumps, discussed in section 6.6.

Overall the yield for module production exceeded the target, which was 90% for each step in the bare module assembly, and the full module assembly and characterization.

7 Mechanical Systems

7.1 Overview

7.2 Barrel Region

7.3 Endcap Region [Version of November 23, 2007]

The active elements of the pixel detector in the two endcap regions are disk sectors, each supporting six modules (three on each side). Eight disk sectors are supported on a disk support ring, forming a disk. There are three disks in each of the two endcaps. The disks in the endcaps are rigidly held by a support frame constructed from carbon composites. This section will describe the construction, survey and testing of the disk sectors (7.3.1), disks (7.3.2) and endcaps (7.3.3).

7.3.1 Disk Sectors

7.3.1.1 Construction

The local support structures (with integrated cooling) for the modules in the endcap region are called disk sectors. The sectors are roughly trapezoidal in shape, and consist of two thin carbon composite sheets with a rectangular aluminum cooling tube and carbon foam in between the sheets. The cooling tube is bent into a W-like shape to fit within the sector, and makes contact with the carbon composite sheets with a compliant, thermally conducting adhesive. Each cooling circuit in the disk region serves two sectors.

[Text here from Gil on the physical construction of the sectors.]

Three modules are mounted on each side of the sector, with the long dimension of the module in the radial direction. The three modules on the back of the sector are rotated 7.5 degrees with respect to the modules on the front side, thus providing full overlapping azimuthal coverage. Figure 35 shows three modules mounted on the front side of a sector.

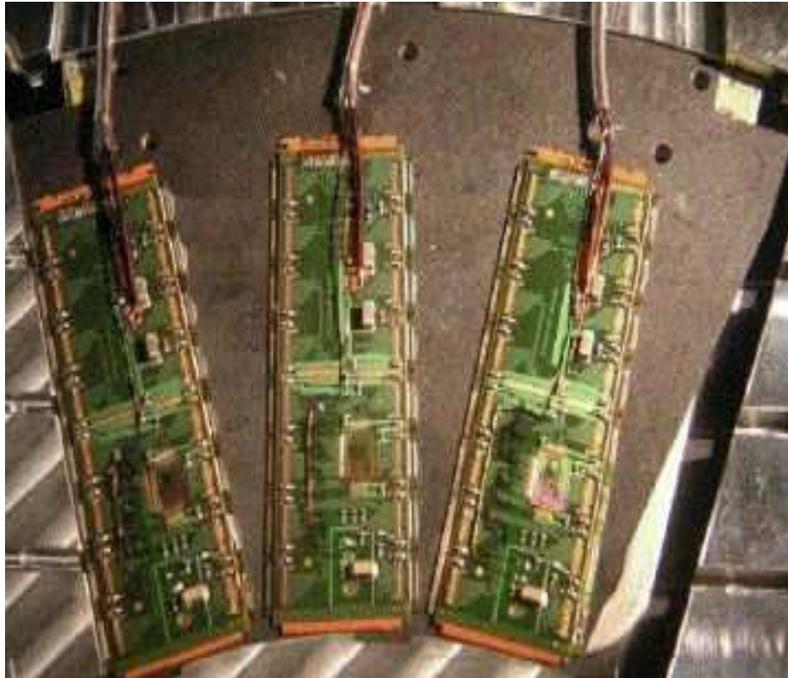


Figure 35: Three endcap pixel modules mounted on the front side of a sector.

The modules are glued to the sectors with Dow Corning silicone SE4445. Nylon filaments of 110 μm diameter are used to control the silicone thickness. During the gluing operation the position of survey

targets in the corners of each module are viewed with an optical SmartScope, to ensure that the modules are placed in the correct positions on the disk sectors. The modules are positioned and glued on each sector with a precision of $2\ \mu\text{m}$ in the plane of the module and about $10\ \mu\text{m}$ perpendicular to the module plane.

7.3.1.2 Sector Survey

After the modules are glued to the carbon surface of the disk sectors, the sector is again mounted on the table of an optical SmartScope. The SmartScope very precisely measures X,Y coordinates (in the plane of the sector) by measuring the position of the table, and measures Z coordinates (perpendicular to the sector) with optical focusing. The SmartScope is used to measure the X,Y position of survey targets at the 4 corners of modules mounted on a disk sector, and these measurements are used to determine the position and orientation of the module in the plane of the sector. The SmartScope also measures 32 X,Y,Z points on the top side of modules mounted on a sector (16 along one long edge, 16 along the other long edge) in the vicinity of the first and last chip ID pads of each front-end chip, and these measurements are used to determine the position and rotations of the module out of the sector plane. The pixel module is treated as a flat rigid plane, as the module distortions (such as bow) are very small.

From the above SmartScope measurements the alignment parameters of each module were calculated in the local module reference frame. The module alignment parameters are those 6 parameters used to describe a flat plane: X, Y, Z, Φ_x , Φ_y , Φ_z . X is the coordinate across the short width of the module, and Y is the coordinate along the long length of the module. In the local module reference frame the module alignment parameters are the displacements of the module from its nominal position (i.e. the difference from nominal). The X,Y, Φ_z alignment parameters calculated from the sector surveys are not the final survey alignment parameters, as they do not include the effect of the placement of the sector on the disk ring. Details about the calculation of the module alignment parameters are given in [69].

In Figure 36 are the distributions of the X,Y, Φ_z module alignment parameters calculated from the sector surveys (treating all the modules as A Disk modules, which means plotting the negative of the actual X and Φ_z values for the C Disk modules), and in Table 8 are the means and sigmas of the Gaussian fits to these distributions. One sees several features:

- The mean of the X alignment parameter distribution is different for front and back modules: $-2.8\ \mu\text{m}$ for front modules, and $+2.8\ \mu\text{m}$ for back modules. This is due to a small systematic offset when the modules were mounted on the sectors. The opposite sign occurs when converting the survey measurements to the same coordinate system.
- The average sigma for the X and Y alignment parameter distributions is $2.0\ \mu\text{m}$, and the sigma for the Φ_z alignment parameter distribution is $0.064\ \text{mrad}$. These resolutions include both the placement accuracy and the measurement precision, and thus represent upper limits on the placement accuracy. These small values show that the modules have been placed on the sectors with excellent accuracy of better than $2\ \mu\text{m}$.

7.3.1.3 Sector Testing

Electrical and thermal tests are performed on the modules after they are glued onto the sectors. The goal is to check any degradation of module performances (early breakdown, increased noise, bump failures, etc.) caused by thermal or mechanical stresses from loading. Another aim is to rank the sectors for disk loading so that the sectors with the least number of bad pixels can be loaded onto the innermost disks. The tests performed on each module are part of the full quality control procedure of the ATLAS

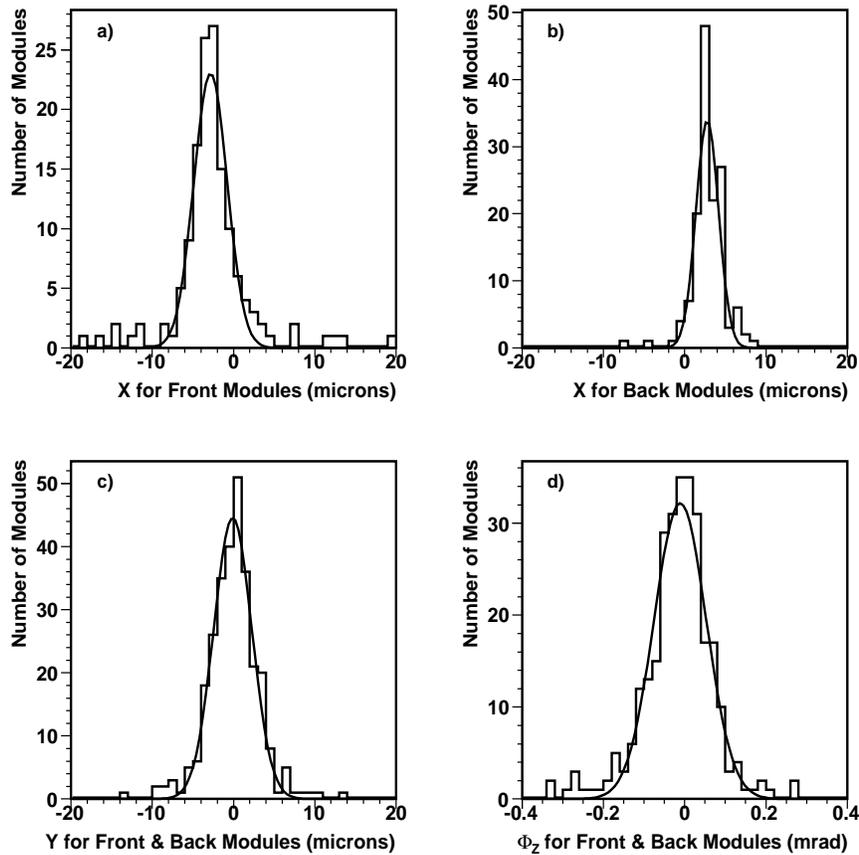


Figure 36: X,Y, Φ_z alignment parameters calculated from the sector surveys.

Pixel Detector and more details are given in [70]. The electrical sector testing sequence consists of the following three sets of basic monitoring scans:

- **LOAD test:** This test is performed immediately after sector loading at room temperature. The test includes I-V, digital, analog threshold, crosstalk and source scans. Data from this test are compared to the single module BURN test (a test performed under similar conditions before the module was loaded on the sector) to observe any changes due to sector loading. All six modules on the sector are tested individually before proceeding to the next test.
- **INBURN test:** During this test the sector is cold soaked for a period of about 12 hours at -30°C with the power off. It is then thermal cycled between -20°C and 20°C ($T_{NTC} = -16$ to 25°C) with the power on. The dwell time at each endpoint is 1 hour and the entire test consists of 14 cycles with about 3.5 hours per cycle. Digital and analog threshold scans are run throughout the burn-in, while monitoring T_{NTC} and digital/analog voltages and currents.
- **STAVE test:** The full electrical characterization is performed after burn-in at operating temperature ($T_{NTC} = -5$ to -10°C) for a fully configured module. The test includes all LOAD scans as well as MonLeak, in-time threshold and GDAC scans. Data from this test are compared to the single module FLEX test to detect any changes due to sector loading or sector burn-in, and serve as the basis for sector ranking.

	Mean	Sigma
X for Front Modules	$-2.8 \pm 0.2 \mu\text{m}$	$2.1 \pm 0.2 \mu\text{m}$
X for Back Modules	$+2.8 \pm 0.1 \mu\text{m}$	$1.4 \pm 0.1 \mu\text{m}$
Y for Front and Back Modules	$-0.1 \pm 0.1 \mu\text{m}$	$2.3 \pm 0.1 \mu\text{m}$
Φ_z for Front and Back Modules	$-0.011 \pm 0.004 \text{ mrad}$	$0.064 \pm 0.004 \text{ mrad}$

Table 8: Results of the Gaussian fits to the sector survey distributions in Figure 36.

Electrical testing and burn-in were performed using one setup. The details of the technical description are given in [71]. The standard module testing hardware chain was used: a PC computer with VME and GPIB interfaces (control cards), ATLAS Pixel TurboDAQ software, a VME crate with a custom board (ATLAS Turbo Pixel Low Level card), an external custom board (ATLAS Turbo Pixel Control Card), GPIB controlled off-the-shelf power supplies, and a LBNL custom designed SURF board with module(s) attached to it. Two surf boards [72] were used to connect all six modules at once. The sector was cooled using an inert fluorocarbon C_6F_{14} running in a secondary loop connected to the sector cooling pipes. Dynalene (HC-50) was used in the primary loop and was cooled using a chiller. The two loops made thermal contact inside a coiled heat exchanger.

The following measurements made during the electrical tests described above were used to rank the sectors: bias current at 150 V, number of bad pixels in digital scans, number of bad pixels in analog threshold scans, number of bad pixels in crosstalk scans, number of bad pixels in in-time scans, number of bad pixels due to bump discontinuity, number of dead or masked pixels measured during source scans, threshold dispersion, and average noise.

The cuts for bad pixels are defined according to guidelines from the ATLAS Pixel Detector collaboration. The above quantities were entered into the Pixel DataBase to maintain a complete record of the production sequence and allow the possibility of tracing any eventual problems. Sector evaluation also considered results from the alignment survey and thermal performance measurements during the electrical tests.

The total number of bad pixels in each of the endcaps can be estimated using the results of the STAVE test performed at the sector level since this is the last, full electrical characterization performed on the modules at operating temperature. It is also the last source scan where bump discontinuity can be accurately measured. Table 9 shows the total number of bad pixels for each of the endcaps, classified by failure. Bad pixels are not double counted: if a pixel is bad digitally, it is not counted as analog bad or source bad.

EndCap	SOURCE	MASK	DIG	ANA	DISC	XTALK	INTIME	TOTAL	%
A	5497	373	5816	471	2559	171	2671	17531	0.26
C	4221	360	52	594	636	127	3131	9036	0.14

Table 9: Number of bad pixels for each endcap, classified by failure. Results are taken from the STAVE test and later connectivity tests.

7.3.2 Endcap Disks

7.3.2.1 Construction

Eight disk sectors are mounted on a 312 mm diameter carbon composite disk support ring, forming a disk. There are three disks in each of the two Endcaps. Each disk has 48 modules, for a total of 288 modules. The radius of the module centers is approximately 119 mm. The inner radius of the active area of the pixel modules is approximately 89 mm. Figure 37 shows one of the completed disks.

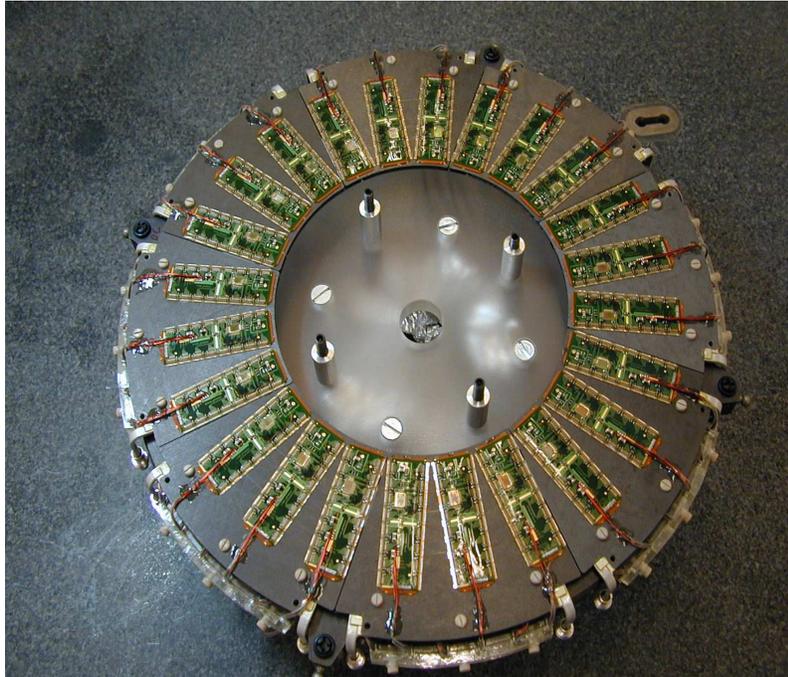


Figure 37: Eight sectors assembled into a disk.

7.3.2.2 Disk Survey

After the disk sectors are mounted on the disk ring, the X, Y positions of the survey targets at the four corners of each front module are again precisely measured with the SmartScope, and are used to determine the final survey position and orientation of the front modules on the disk with a precision of a micron. The back modules are not surveyed after mounting the sectors on the disk, but the measurements done after mounting the modules on the sectors are used to calculate the positions of the back modules on the disks with a precision of about 5 microns.

The final X, Y, Φ_z alignment parameters of the modules were calculated from the disk survey SmartScope measurements in a manner similar to the way they were previously calculated for the sector survey measurements. These final X, Y, Φ_z alignment parameters are the displacements from nominal due to both the placement of the modules on the sector and the placement of the sectors on the disk ring.

In Figure 38 are the distributions of the final X, Y, Φ_z module alignment parameters calculated from the disk surveys (treating all the modules as A Disk modules, which means plotting the negative of the actual X and Φ_z values for the C Disk modules), and in Table 10 are the means and sigmas of the Gaussian fits to these distributions. One sees several features:

- The average sigma for the X and Y alignment parameter distributions is $12 \mu\text{m}$, and the sigma for the Φ_z alignment parameter distribution is 0.130 mrad . These values include both the placement of the modules on the sector and the placement of the sectors on the disk ring. Recall from the sector

survey results (which only include the placement of the modules on the sector), that the average sigma for X and Y was $2.0 \mu\text{m}$, and the sigma for Φ_z was 0.064 mrad . Thus we see a much larger variation in the module position due to the sectors being placed on the disk ring than due to the modules being placed on the sector.

- The mean of the Y alignment parameter distribution is $35 \mu\text{m}$. The local module Y direction is the radial direction in the disk. The reason that the Y alignment parameter is so large is mostly because the average radius of the mounting holes in the disk rings is larger than the nominal value of 156 mm . From independent disk ring measurements, the radius appears to be roughly $25 \mu\text{m}$ larger than nominal. This accounts for the major part of the $35 \mu\text{m}$.

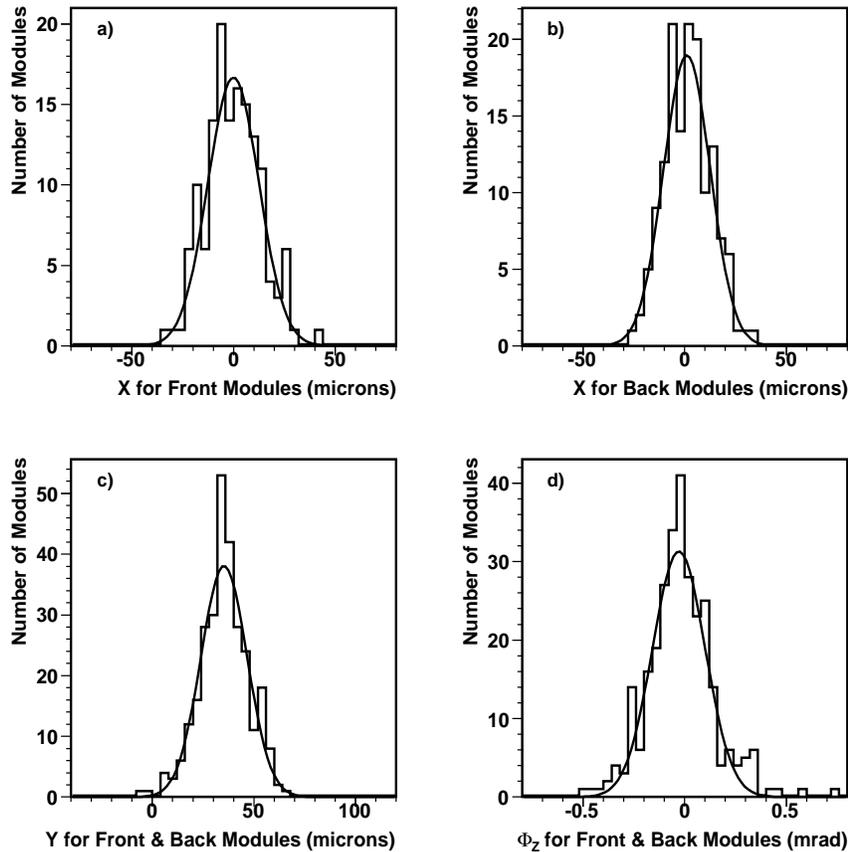


Figure 38: Final X,Y, Φ_z alignment parameters calculated from the disk surveys.

	Mean	Sigma
X for Front Modules	$-0.1 \pm 1.1 \mu\text{m}$	$12.6 \pm 0.9 \mu\text{m}$
X for Back Modules	$1.1 \pm 1.0 \mu\text{m}$	$11.5 \pm 0.8 \mu\text{m}$
Y for Front and Back Modules	$35.3 \pm 0.7 \mu\text{m}$	$11.4 \pm 0.6 \mu\text{m}$
Φ_z for Front and Back Modules	$-0.029 \pm 0.008 \text{ mrad}$	$0.130 \pm 0.009 \text{ mrad}$

Table 10: Results of the Gaussian fits to the disk survey distributions in Figure 38.

7.3.2.3 Disk Testing

After the sectors were mounted on a disk ring, a continuity test was performed on the modules. Its purpose was to quickly check that the delicate module circuitry survived the mounting operation and any sector or disk handling. Since it was done without cooling, at room temperature, the modules were powered on a chip-by-chip basis, one-at-a-time, and only for a short time. The continuity test was performed as each sector was mounted on the disk ring, and again upon the disk completion. It took about 5-10 minutes per sector.

An electrical test was then done after the continuity test. The purpose of the electrical test was to check that no subtle changes occurred during the mounting of the sectors on the disk ring, and to verify the stable performance of all modules. The electrical test was a shorter version of the LOAD test done during sector testing, and it involved the following scans:

- MCC scan: This is a test of the MCC operation and connectivity.
- Digital functionality: This scan checks all registers (global and pixel front-end) and all buffers using digital injection to test full overflow conditions. It tests all pixels with digital injection (digital inject scan). This must be done with nominal VDD voltage at 40 Mbps single link, 80 Mbps single link, 40 Mbps dual link, and 80 Mbps dual link.
- Analog functionality: This is the most time-consuming and complex set of scans performed with the bias voltage on. It is a sequence of operations and scans needed to certify proper analog behavior: threshold tune using internal injection to set a uniform threshold along the module, internal injection threshold scan (measures threshold and noise of each pixel using internal injection), FDAC tune and test, ToT tuning (tune the ToT response to a MIP signal for each pixel in order to have a uniform response to the collected charge in a time acceptable for operation in ATLAS; it calibrates the relationship between the measured ToT and collected charge), and the cross-talk scan to measure the cross-talk fraction and to detect bump defects resulting in increased capacitive coupling between pixels.
- Noise occupancy: This test consists of enabling one front-end chip at a time in self-trigger mode and measuring the rate of hits. Whereas pixels that generate hits at a rate greater than 1 Hz (1 kHz) are tagged as hot and are disabled in the slow (fast) mask during module and sector testing, it is not the case during disk testing. Here we only record their total number and compare these results with noise scans performed during sector testing.

A sensor bias voltage measurement was performed after the electrical scan was finished because we could not control the relevant power supply from the ATLAS TurboDAQ program. The bias voltage was ramped up to 600 V in 10 V increments to check for possible sensor damage. The current stability at different bias voltages was investigated over a period of more than 15 minutes.

7.3.3 Assembly of Disks into Endcaps

7.3.3.1 Construction

To assemble each endcap, three disks were rigidly supported by four mounts within a lightweight, octagonal, carbon composite support frame, shown in Figure 39.

Figure 40 shows a perspective cut-away view of the pixel detector. The view shows individual barrel and endcap modules, supported with their associated services on staves and disks within the octagonal support frame.

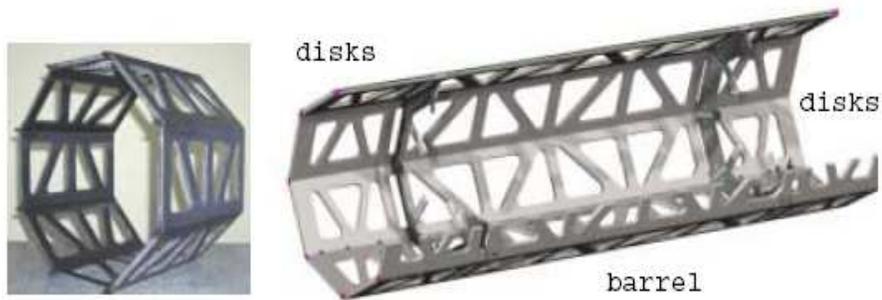


Figure 39: Carbon composite support frames.

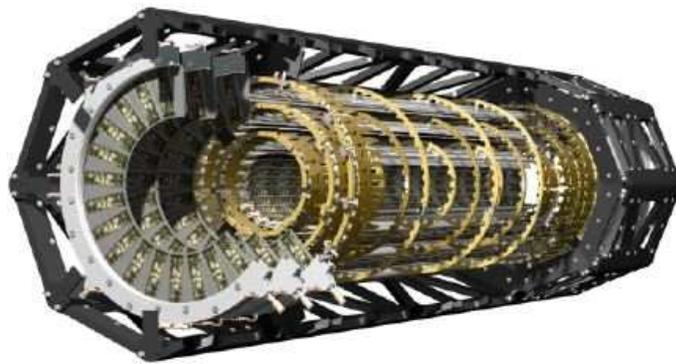


Figure 40: A perspective cut-away view of the pixel detector..

7.3.3.2 Endcap Survey

No surveys were done of the modules or sectors after the disks were assembled into an endcap, since the relevant fiducial marks were not viewable at that point.

7.3.3.3 Endcap Testing

All cooling circuits on both endcaps were leak checked down to $1 - 4 \times 10^{-9}$ Torr. This is the value required by the evaporative cooling system.

A connectivity test of the endcaps was performed at various stages of the integration to ensure that no modules were damaged during handling or transport. A connectivity test consists of a series of basic functionality checks performed chip-by-chip with no cooling. Each module is powered briefly and the digital, analog and bias voltages and currents are measured and compared to a set of standard values. A MCC scan is then performed as well as FE chip register/receiver tests. Each FE chip is configured to measure voltages and currents, which are compared to expected values. Finally, a short threshold scan is performed with and without bias voltage to verify that the high voltage is properly delivered to the module. The total testing time required for one endcap is two days.

A connectivity test was performed on both endcaps after loading, but before shipment to CERN.

The connectivity test was repeated after delivery of the endcaps to CERN to verify that no modules were damaged during the transport. Testing of Endcap C at CERN showed no failures on any of the

modules. Endcap A showed no failures at CERN other than the three failures reported before shipment. An additional connectivity test for Endcap C was performed after integration into the Pixel Package. The test found one module with missing high voltage due to a weak bond on the module. The bond was repaired by adding silver epoxy to the high voltage hole.

Since Endcap A was used in a system test at CERN, an additional connectivity test was performed before any further integration to check for any damage to the modules during the system test or during handling in preparation for the system test. There were several modules found with intermittent HV failures. These problems were fixed by re-soldering the HV pins on the ELCO connector, by adding solder to HV wire connections, by adding silver epoxy to HV bonds, or by reinforcing glue tacks.

Gil: The parts *emphasized* may have already be written by other authors of the pixel paper?

The ATLAS pixel detector consists of a barrel and two endcap parts. The barrel part is built up of 3 layers (B-layer, layer 1, and layer 2) surrounding the interaction point and the beampipe. There are 3 disks per endcap. Each barrel layer has a certain number of staves (B-layer 22, layer 1 38, layer 2 52 staves) where the modules are mounted on. These modules register the information of traversing particles and they are read-out via optical fibers. Modules are also mounted on the forward disks. A module transfers the data information from the detector to the electronics in the counting room by using one (or in the case of the B-layer two) optical fiber(s), while the timing information to read-out a module goes via an additional optical fiber from the counting room to the detector. There are 13 modules per staff, and 48 modules per disk. The total number of modules is 1456 for the barrel part (B-layer 286, layer 1 494, layer 2 676 modules), and 288 modules for the two endcaps, i.e. there are 1744 modules in total.

7.5 External Services

External services are the ones outside the thermal shield/Faraday cage (or PP1, fig ??) up to the counting rooms. The power supply system has been designed to balance between high granularity and cost. The compromise has been achieved keeping individual power lines, but grouping them to the power supplies channels. Each sector or halfstaff will have all the similar bias line powered by a single channel of the power unit. For the HV, a single power supply channel will power 6/7 modules, respectively for sector or halfstaff. The power supplies are located in the counting rooms to have easier access during operation and commercial units can be used, since the magnetic field and the radiation dose are negligible there. The acceptable voltage drop along the power lines is one of the critical parameters. Several patch panels are acting as break points between the different cables types with increasing diameter towards the counting rooms. The design of the external services has also been driven by the need of integration with the pixel cooling tubes and all other ID services in the assigned volume. A detailed description of all the services can be found in [?].

In fig ?? a schematic of the different services routing and locations of the break points are shown. All the services have to be disconnected at PP1 to allow for removal/installation of the pixel system. All the services up to the tile fingers follow the same routing, beyond this point the services are split into two groups:

- all cables (including those for the PST active insulation) and optical fibers power will make a dogleg coming out of the first layer of muon chambers and then running towards the ATLAS central crack ($z=0$) in between the first and second layer of muon chambers.
- cooling tubes and N2 lines will go along the calorimeter outer surface toward $z=0$.

While at PP0 and PP1 all the cables and cooling connections are located close together in the same area, PP2 and PP3 for cables, fibers and cooling tubes are placed in different locations because they

are subject to different requirements. In general the component used between P1 and PP2 have to be radiation resistant (up to 5×10^5 Gy), while the more external components use standard material¹¹⁾

Optical links

The architecture of the optical data links for the ATLAS Pixel Detector is divided into an on-detector and off-detector side. The on-detector side includes all devices placed within the ATLAS detector, whereas the off-detector side consists of all parts placed onto the read-out driver (ROD) outside the detector. The on-detector optical link is situated at patch panel 0 (PP0), and all off-detector components are sitting in counting room USA15. At PP0 are installed the so-called opto-boards, on which by different electronics components (VCSEL and PiN packages) the electrical digital signals are converted into light and vice versa. The connection inside the pixel detector between PP0 and PP1 is done by 8-way optical fiber ribbons, while the connection outside the pixel detector between PP1 and USA15 is done by optical unitube fiber cables which contain eight 8-way ribbons each. For installation in and removal from the ATLAS cavern, all services of the pixel detector must be disconnected at PP1. Though there are 8 single fibers in a ribbon out of these only 6 or 7 fibers are actually used for transmitting data from the modules or receiving TTC information for the modules.

The total number of single fibers for the pixel detector is 3774. The inside of the ATLAS detector is a zone of high radiation limiting the lifetime and the light transmission of optical fibers. Outside the ATLAS detector the radiation levels will be considerably lower to the ones inside. Therefore radiation hard Fujikura SIMM50 multimode fibers are used inside the ATLAS detector and radiation tolerant Draka GRIN50 fibers for timing and GRIN62.5 fibers for data transfer outside of the detector. Only the B-layer reads out the data information with 2 optical fibers and receives 1 timing (TTC) signal per module, all other modules are read-out by 1 data and receive 1 TTC fiber.

The whole pixel detector with its 3 layers and 6 disks has 272 opto-boards with 316 VCSEL and 272 PiN packages on-detector. Each of these packages is connected at PP0 via a pure ferrule of a MT8-connector without any connector housing to an 8-way radiation hard SIMM optical fiber ribbon connecting PP0 with PP1, which is located at the end of the pixel support tube. Two 8-way ribbons coming from PP0 will go into a MF16 (MF-A1/MT16) connector which fits into the custom made PP1 connector plate. Due to the different inner and outer service panels there are (including spares not integrated in the detector) 494 “long” (251.0 cm) and 246 “short” (226.0 cm) nude, non ruggedized ribbons. The eight PP1 connector plates (1 per quadrant of side A and C) incorporate the MF16 connectors of the 320 double ribbons.

80 optical unitube fiber cables transfer the data and timing information between PP1 and the counting room in USA15. The unitube cable has a protective sheath of halogen free flame retardant polyethylene (HFFR-PE) and its sheath has marks to indicate being an optical cable. In addition there are 2 fiber cables per side being installed as spares in the cavern but these are not connected to the PP1 endplate and the USA15 electronics. The 84 fiber cables consist each of 8 about 8.1 m long radiation hard SIMM50 ribbons which are fusion-spliced to 8 about 70.3 m long radiation tolerant GRIN50/62.5 ribbons. The total length of the spliced joint is about 60 cm and over this length the cable diameter is growing from 0.95 cm to 1.4 cm. The technique of splicing avoids having any additional patch panel for the optolink, and there is the advantage that splicing is cheaper and more reliable than connectors. Both SIMM50 and GRIN50/62.5 cable ends are prepared by carefully removing the outer sheets, for the SIMM50 (PP1) end about 100 cm with 4 MF16 connectors, and for the 70.3m GRIN (USA15) end about 300 cm with 8 SMC XL multi-fiber connectors based on the MT ferrule, in order to make possible an easy connection to the PP1 endplate and to the electronics in the counting room USA15. In total there are 3 different flavours of optical cables with 8 ribbons each: 40 yellow data SIMM50/GRIN62.5, 32 blue TTC SIMM50/GRIN50,

¹¹⁾PPF1 is not a break point for the pixel services, used to identify the cryostat bore end corner region.

and 12 grey “hybrid” cables with 4 ribbons each of the the data and TTC type.

All PP0 \leftrightarrow PP1 ribbons and all 84 optical fiber cables were tested at the factory in a similar configuration than the installation configuration in the ATLAS detector. Light was injected at the ferrule (PP0) end of the ribbon and detected at the SMC XL (USA15) end of the fiber cable. This method measures hence the losses of the two connections at PP0 and USA15, of the fiber connector plate, of the fiber length, and of the splice. The attenuation of the light signal was for the data transfer always smaller than 2.5 dB, and for the TTC transfer smaller than 3.5 dB. The light attenuation of the PP0 \leftrightarrow PP1 ribbons alone with the two connector types at their ends was smaller than 1.0 dB. After installation of the optical fiber cables in the ATLAS cavern all 84 cables with their 672 ribbons were tested with an optical time domain reflectometer (OTDR) in order to guarantee that no fibers were damaged during cable laying and fixation in the electronics racks.

HV system

Pixel High Voltage cables do not have break points and go fromPP1A to the counting rooms. Due to the connector choice at PP1 (to be explained by Jose or here) the HV cable is in reality a “bundle” of four round shaped cables [3]. The individual cable is made of 7 twisted pairs of AWG26 conductors, SILTEM insulated and rated for use at 700V. SILTEM is a flexible siloxane-polyetherimide polymer, non-halogenated, that is used for cable coating and has been recently qualified as radiation resistant at a level higher than the 5×10^5 Gy foreseen at PP1. [siltem-STM1500 ULTEM GE]

The cable bundle is terminated at PP1 with a 64 pin LEMO Series 5F (FGW.5F.364.XLC) connector (check gender) and at the other end with a 22pin LEMO/REDEL Rectangular High Voltage Connector standard at CERN (SCEM 09.41.34.110.8 22 pins). In total 336 cables, including xxx spares, equally split between US and USA are installed. At the beginning of the operation phase 6/7 modules will be operated from a single power supply channel, but the silicon radiation damage during operation will increase leakage current above the power supply channel specification and the modularity of HV system should be changed. To accommodate this possibility and to introduce a current measurement for each single module, a dedicated unit (HV-PP4) has been introduced prior to the HV unit. Each HV-PP4 crate will monitor up to 117 detector module currents, in the range 0,4—4 mA. 16 crates will be installed. The commercial 16 channel HV unit used is a product of iseg (Rossendorf, Germany) (EHQ-F007n-F). Each channel provides 4mA, up to 700V, coating. Each unit is remotely controlled and has interlocking capability for the individual channels. In the initial configuration 24 units will be installed.

LV system

The LV distribution system is more complex of the HV one. To protect the integrated circuits, that are manufactured in deep sub-micron CMOS technology, against voltages surges or spikes a remotely programmable regulation station capable of providing individual floating power output with low ripple has been designed. The station is >10m apart from the detector (PP2 region), and each FE line is continuously ‘sensed’ down at the module to promptly adjust the output voltages.

One regulation station can power up to 84 modules (V_{dda}, V_{dd}, V_{Vdc}) and communicate with the ATLAS Detector Control System via a CAN bus interface. The core of the regulation station are 12 printed circuit boards, Regulator Boards, built on a highly dissipative substrate (approx 10W/board). Each board houses 16 ST rad-hard voltage regulators (LHC4913+) and provide about 1A at 2V with 10mV regulation step. The line devoted to V_{Vdc}, that is provided for one optoboard, has 100% redundancy. The board has the ability to digitally adjust the output voltage and to monitor voltages and currents via a precise double slope ADC. The controller board is based on a FPGA (ACTEL APA075). The full system has been irradiated and is rad-tolerant upto NIEL > 10^{12} 1MeV n_{eq}/cm^2 . The mechanical structure of the regulation station is completely enclosed in mechanical panels to ensure proper shielding and is kept at

18 C with a dedicated C6F14 circuit, manned with the similar circuits of SCT and ID cable cooling [?]. The unregulated input voltages enter the box via an Inpt board, are distributed by the backplane to the regulator boards and after being regulated are grouped to provide all the necessary lines for one halfstave or sector . LV Type II and Type III cables have consequently different structures.

28 regulation stations are distributed in 12 different location near the first layer of muon chambers, mounted in group of 2 or 3 crates. Each group of crate is connected to the cooling system , is sensed by a sniffer fire alarm system [?], and is inserted in the Pixel Interlock Safety System.

An LV Type II cable is a bundle of tree round cables of different structure. Two cables (VDD, VDDA) have 7 twisted quad of (2xAWG20, 1 xAWG22, 1 AWG28) multicore conductors. The third cable, VVDC, has 1 twisted quad of (3 xAWG22, 1 AWG28). They are SILTEM insulated and shielded. The bundle is DC grounded at PP1 side and AC grounded at PP2 side. The cable bundle is terminated at PP1 with a 64 pin LEMO Series 5F (FGW.5F.364.XLC) connector and at PP2 with a 66 pin amagnetic Positronic connector (GMCT66M00P0Z0). In total 276 bundles , including 4 spares, equally split between US15 and USA15 are installed.

LV Type III cables are individual cables with standard insulation. VDD (VDDA) cable has 7 twisted pairs of AWG16 (AWG14), while VVDC has one twisted pair AWG18. VDD (VDDA) cable is terminated at both side with a V34 connector (Positronic GMCT34M0TLR00), VVDC is terminated at both end on a 9pin Sub-D connector.

As for the HV power distribution system, a patch panel (LV-PP4) is added before the LV units to accommodate the different modularity and to provide additional current measurements. LV-PP4 are built using ELMB's. Opto insulated circuit measures with a 10mA precision up to 2A. Each LV-PP4 handle up to 28 channels and a total of 3500 channels will be installed.

The commercial 12 channel LV unit used is a product of W.IE.NE.R. (Burscheid, Germany) (PL512). Each channel provide 15V, 10AV, coating . Each unit is remotely controlled and has interlocking capability for the individual channels. 24 units will be necessary to provide VDD and VVDA to the detector. VDDC is supplied by the SC-olink together with other signals needed for the optoboards.

SC-Olink and monitoring system

For the optoboard , a custom supply (SC-Olink) to provide two low current channels has been developed [?].

Type II and type III NTC, OOPTO , ENV cables

Cooling tubes

xxxx.

8 Test Beam Studies

The performance of the Pixel detector modules has been measured systematically in beam tests throughout their development. Initially, sensor properties were studied with single chip assemblies, namely reduced size sensors which were read out by a single front-end chip. Later, full Pixel modules were analyzed in test beams. Results from test beams can be found in [73–84]. In this section we summarise beam measurements performed using the ATLAS pixel modules during final stages of development and qualification.

8.1 The Test Beam Setup

Test beam measurements were performed at the H8 beamline of the Super Proton Synchrotron (SPS) at CERN, using a beam of 180 GeV charged pions. A beam telescope [85] was used to track beam particles independently of the devices under test. The telescope consisted of four planes of double-sided silicon strip detectors, with perpendicular strips at 50 μm pitch, that provided a reference track with an extrapolation uncertainty of about 6 μm . Pixel assemblies under test were placed between the second and third strip planes. Irradiated modules were inserted into a thermally insulated box, which maintained a temperature of about -7°C , as foreseen in ATLAS.

A trigger was provided by the coincidence of three fast scintillators. For each event, a TDC measured the difference in time between the particle passage and the edge of a 40 MHz clock, seen by the pixel electronics. For each trigger, data from eight consecutive cycles were readout in order to study the pixel signal behaviour in a 200 ns window.

For a fraction of the data taking, a high intensity beam was provided by the CERN SPS in order to study the efficiency of the readout architecture when the particle rate was comparable to that expected for the B-layer at the design luminosity of the LHC, namely $10^{34} \text{ cm}^{-2}\text{s}^{-1}$. In the beam center, the flux reached approximately 10^8 particles/cm²/s. At this particle flux, both the scintillator system and the microstrip telescope were inoperable. Data were instead collected with a random trigger and particle trajectories were reconstructed using four pixel modules.

8.2 Irradiation of Tested Assemblies

A major design concern for the Pixel detector is radiation tolerance during the lifetime of the experiment at the LHC. Single chip assemblies and modules were systematically irradiated before operation at the test beam with 24 GeV/c protons at the proton irradiation facility at the CERN Proton Synchrotron (PS) accelerator. The proton fluence was $2 \cdot 10^{15} \text{ cm}^{-2}$, corresponding to a 1 MeV neutron equivalent fluence of $10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ and a dose of about 500 kGy. This corresponds to the expected dose resulting from 5 years of LHC operation at $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ luminosity located at the B-layer position. Throughout the irradiation, subsequent storage and test-beam operation the modules were kept at about -7°C . Unless otherwise specified, the irradiated modules were operated at 600 V in the test beam, while the un-irradiated ones were operated at 150 V.

8.3 Event Reconstruction and Analysis

Tracks were reconstructed using information from the telescope microstrip detectors only (except during the high rate tests), in order to have an unbiased extrapolation of the tracks through the pixel detectors under test. Events were selected [86] with one and only one track reconstructed by the silicon microstrip telescope. Tracks were required to extrapolate to a fiducial region inside the pixel sensors (at least 40 μm from the edges of the detector). In addition, only events with a track fitting probability greater than 0.02 were kept. For each selected event, the intersection of the trajectory of the beam particle with the pixel detector was calculated.

Neighboring pixel cell hits were clustered together. The bunch crossing identifier of the earliest pixel hit in the cluster was assigned to the whole cluster. Cluster position was reconstructed as the geometric mean position of the pixel cell centers ¹²⁾.

¹²⁾For the measurement of spatial resolution, the cluster position was reconstructed with a charge interpolation algorithm.

8.4 Measurements of Detection Efficiency

The efficiency was computed requiring a pixel cluster near the intersection of the trajectory of the beam particle with the pixel detector and in the expected bunch crossing. The width of the window used to associate a cluster to a track was ± 0.2 mm along the short pixel side direction and ± 0.4 mm along the long pixel side direction.

The efficiency was computed as a function of the time $t = t_0 + n \times 25$ ns where t_0 is the TDC phase between the trigger and the edge of the clock operating the modules, and n is the bunch crossing ID of the cluster. Efficiency curves at perpendicular beam incidence are shown in Figure 41 for an un-irradiated module (left) and for a module irradiated to 10^{15} n_{eq}cm⁻²(right).

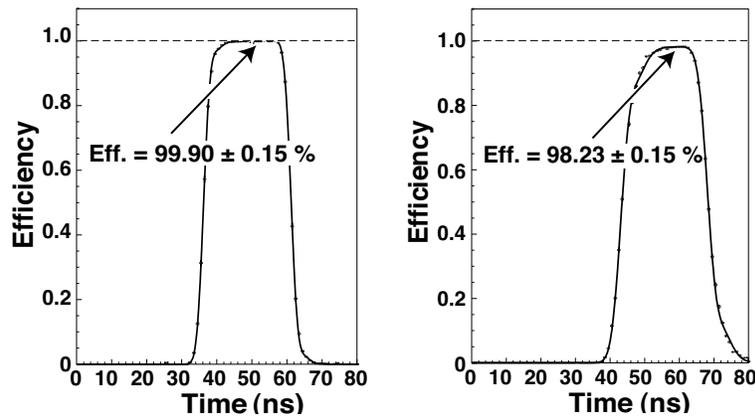


Figure 41: Detection efficiency ϵ at perpendicular beam incidence as a function of particle arrival time for an unirradiated module (left) and for a module irradiated to 10^{15} n_{eq}cm⁻²(right).

At the LHC, only hits with a time stamp associated with a level 1 trigger are readout, i.e. only hits for which the leading edge rises in the 25 ns window corresponding to the clock cycle associated to the trigger are recorded. The position of this window can be tuned by setting the delay of the clock edge with respect to the bunch crossing time. The timewalk, i.e. the delay between the particle crossing and the leading edge of the signal passing the discriminator threshold, results in a spread in the time when hits are generated. It is therefore important to find the delay of the clock edge that maximises the number of hits collected within one clock cycle. Moreover, the performance should be stable for small variations of this delay and therefore a plateau in the relationship between efficiency and time delay is required.

A good detector should have a high efficiency for a significant range of clock phases. For the unirradiated detector of Figure 41 (left), the plateau efficiency was 99.90% and this value was maintained for about 14 ns (plateau width). For the irradiated detector of Figure 41 (right) the efficiency decreased to 98.23% but was still well above the ATLAS Pixel module specifications for efficiency ($\geq 97\%$). The timing characteristics were affected by irradiation, resulting in slower rising and falling edges, leading to a narrower efficiency plateau. However, the rise time was only slightly degraded by irradiation and a large plateau was still obtained, with a width of about 9 ns.

A summary of measurements performed on several ATLAS Pixel production modules is given in Table 11, for data collected at normal incidence. The detection efficiency was 99.9% for an unirradiated module, while for the irradiated modules it varied from a minimum of 96.4% to a maximum of 98.4%, with an average and r.m.s of 97.8% and 0.7%, respectively. All irradiated modules had similar timing constants. The width of the efficiency plateau for the irradiated detectors was (9.7 ± 1.1) ns. No statistically significant difference was observed between the two sensor producers or the two bump-bonding techniques.

For each module, the efficiency losses were reported separately when due to missing hits (0-hits) or due to timing losses (out-of-time or late hits, i.e. hits recorded in subsequent bunch crossings). These hits cannot be assigned to the track and thus are a source of inefficiency. Two thirds of the efficiency losses, $(1.5 \pm 0.4)\%$, were typically in the 0-hits class and the rest $(0.7 \pm 0.3)\%$ in the timing loss class. Missing hits were due to various reasons: pixels not giving a signal at all (in turn due to detached bumps), noisy pixels masked at the readout (see below) and pixels collecting a signal lower than threshold. This last cause of efficiency loss as well as timing losses in irradiated detectors were related to regions of poor charge collection located near the bias grid [77]. The bias grid is a metallic line used to ground the pixel side of the sensor before connection to the front-end electronics, which was necessary for ensuring quality controls performed on the sensors before bump-bonding.

module	510332	510337	510689	510704	510823	510852	510910	510929
irradiated	YES	NO						
sensor producer	ON	CIS	ON	CIS	CIS	CIS	CIS	CIS
bonding	indium	indium	indium	indium	solder	solder	indium	indium
efficiency (%)	97.7	98.4	96.4	98.2	98.4	98.0	97.4	99.9
0 hits (%)	1.4	1.1	2.3	1.3	1.2	1.4	1.6	0.0
late hits (%)	0.9	0.5	1.3	0.5	0.4	0.6	1.0	0.1
plateau (ns)	8.6	9.2	8.5	9.3	10.2	11.4	10.8	13.9
masked (%)	0.0	0.1	0.0	0.0	0.3	0.0	0.0	0.0

Table 11: Summary of the pixel efficiency measurements performed at normal incidence with the standard bias voltage (150 V for modules without irradiation and 600 V for the irradiated modules). The first row provides the module identifier, the second whether it was irradiated before operation at the test beam, the third the producer of the sensor, the fourth the bump-bonding technique. The subsequent rows report the detection efficiency, the fraction of losses due to undetected particles (0 hits), the time-walk losses (late hits), the width of the efficiency plateau and the fraction of pixels found noisy in the offline analysis (excluded from the efficiency analysis).

8.4.1 Noise

Noisy pixels, identified prior to the test beam, were masked in the front-end chip configuration file. This procedure introduced an inefficiency which contributed to the 0-hit class.

In addition, a few noisy pixel cells were also detected and masked during the offline reconstruction [79, 83], using the following procedure. In any given run the level-1 timestamp of pixel hits, correlated with a trigger, had a well defined value l_0 . In order to search for noisy pixel cells, hits with a level-1 either happening before l_0 or far after the most probable value l_0 ($l < l_0 - 1$ or $l > l_0 + 3$) were selected. If a pixel cell contributed either to more than three times to these events or for a fraction larger than 10^{-5} of the total number of events, then it was tagged as noisy and masked.

The track extrapolation was required to be at least $50 \mu\text{m}$ away from the pixel cells masked during the offline reconstruction. Thus the pixel cells masked by the offline reconstruction did not contribute to the inefficiency. The number of noisy cells was however very small. With the procedure described above, only 2 noisy pixels (out of 47232 i.e. 4×10^{-5}) were found in the unirradiated module. For all but one of the irradiated modules, the number of noisy, masked, pixel cells ranged from 0 (for three modules) to 32. One exceptionally noisy module (510704) had 129 noisy pixels, still only a fraction, 0.3% of the total number of pixels.

8.4.2 Timing Studies

In ATLAS the clock phase can be adjusted for each individual Pixel detector module, but it is the same for all the pixels of a module. Hence in order to achieve a good efficiency it is important that the timing differences (i.e. the spread of the t_0 values of the efficiency curve) between different pixels of a module is smaller than the width of the efficiency plateau. The timing differences between different types of pixels (ganged, long and standard) and between the 16 front-end chips of a module were found to be smaller than 2 ns (see Table 12). Since this difference is smaller than the width of the efficiency plateau, it should have a negligible effect on the module efficiency at the LHC.

pixel type	standard	long	ganged
ϵ (%)	98.0	99.1	97.7
t_0 (ns)	11.7	12.4	13.7
plateau (ns)	11.7	10.8	11.3

Table 12: Detection efficiency and timing parameters measured for different types of pixels (standard, long and ganged, see chapter ?? for their description) for a module irradiated to 10^{15} 1 MeV $n_{eq}cm^{-2}$.

8.4.3 Detection Efficiency and Bias Voltage

The in-time efficiency for an irradiated module is reported in Figure 42 (left) as a function of operating bias voltage. For low values of bias voltage, the collected charge is small since the detector is not fully depleted. Hence the maximum efficiency is smaller. The effect of time-walk is also evident: when the collected charge is smaller, the hits are detected later and the efficiency curve moves to the right. The lower amount of collected charge affects also the timing characteristics of the module. As much as the detector bias voltage decreases, then less charge is collected, the module shows clearly slower rising and falling edges. As a consequence, the efficiency plateau is much narrower. The peak efficiency is reported as a function of the bias voltage in Figure 42 (right) for two modules irradiated to 10^{15} $n_{eq}cm^{-2}$. In agreement with the results on the collected charge, full efficiency is reached at 500 V when the detector is fully depleted.

8.4.4 Detection Efficiency and Incidence Angle.

In ATLAS, tracks will not generally be perpendicularly incident on the Pixel module plane. Consequentially, the influence of incidence angle on module performance needs to be evaluated. When particles traverse the detector at an angle, the charge released in the sensor is spread over a larger area and is usually divided among more than one pixel cell. This has two competing effects on the detection efficiency.

Because of charge sharing, each individual pixel has a lower signal. This increases the hit losses due to the time-walk.

As discussed above, at normal incidence most of the hit losses occur when the particle transverse the detector in a spatially limited region of the pixel cell. This region is close to the edge between two pixel cell, where the bias grid is located. In this region charge sharing occurs also at normal incidence because of diffusion, and the charge collection efficiency is low. When the particle incidence angle is in the range of 10° , the charge released in the sensor is spread over a length much larger than the region with poor charge collection, so that the overall charge collection efficiency is higher.

Table 13 presents the detection efficiencies for particles at 0° and 10° for both irradiated and unirradiated modules. The results indicate that the spread of charge over a larger region actually dominates

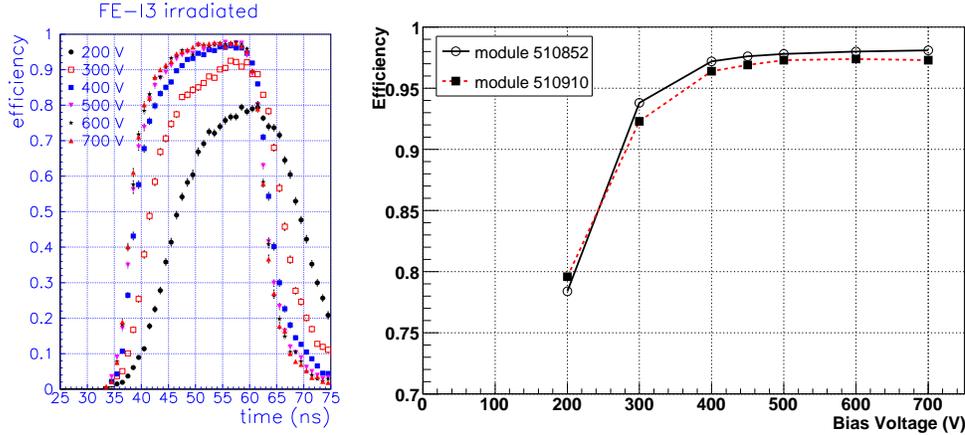


Figure 42: (left) Detection efficiency as a function of time in ATLAS Pixel modules irradiated to $10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$, for different values of the operating bias voltage. (right) Maximum detection efficiency as a function of operating bias voltage in ATLAS Pixel modules irradiated to $10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$.

so that the efficiency is larger when the detectors are tilted. The results reported in this paper, which are mostly obtained with measurements at normal incidence, are thus conservative.

module	510852	510910	510929
normal incidence	98.0%	97.4%	99.9%
10°	98.4%	98.5%	>99.93%

Table 13: Detection efficiency measured for the unirradiated module 510829 and the irradiated modules 510852 and 510910, at two values of incidence angles.

8.4.5 Efficiency in a High Intensity Beam

Beam tests of ATLAS Pixel Detector production modules were performed with a high intensity pion beam at various beam intensities, up to the value foreseen for the innermost pixel layer at the design LHC luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$, in order to test the readout system in high occupancy conditions. At each intensity data were taken with different configurations of the front-end chip. In fact, there are several mechanisms which can induce hit losses, dependent on the rate of particles crossing the detector:

- If additional charge is deposited while the discriminator is above threshold, it is added to the initial one and the second hit is lost;
- After the discriminator goes below threshold, the pixel cell is still unable to accept new hits until the sparse scan logic has transferred the hit data to the end of column memory buffers;
- Finally, if all the memory buffers are occupied when the hit is transferred, it is lost due to lack of memory space

The first effect depends on the local occupancy of the pixel cell, i.e. the probability to get a hit in a bunch crossing, and on the average ToT response for a charged particle.

The other effects are sensitive to the hit rate per column pair, since all pixel cells in a column pair share the same sparse scan logic and memory buffer. Therefore results are quoted as a function of the occupancy per column pair (cp) per bunch crossing (bx). The expected occupancy ¹³⁾ for the innermost layer at the LHC at $10^{34}\text{cm}^{-2}\text{s}^{-1}$ is 0.17 hits/cp/bx, which is approximately equivalent to 10^8 hits/cm²/s, with an average multiplicity of 1.5 hits per track. At the test beam the pixel detection efficiency was studied for the entire range of occupancies expected at the LHC and beyond.

The summary of efficiency measurements are reported in Table 14 with indication of the maximal occupancy per column pair. With standard front-end electronics settings, the detector efficiency of irradiated detectors remains unchanged and close to 98% up to an occupancy of 0.24 hits per clock cycle per column pair. This value exceeds by about 40% the maximum occupancy foreseen.

At larger occupancies, a small inefficiency arises from saturation of the end-of-column buffers of the front-end electronics chip. This saturation is properly flagged by the FE Buffer Overflow flag. Removing the events with the error flag restores the hit efficiency to its value at a lower intensity. The maximum value of column pair occupancy reached at the test beam was 0.27 hits per clock cycle for irradiated modules, and 0.30 hits per clock cycle for the not irradiated module. The corresponding efficiencies were about 96% for irradiated modules and 89.8% for the not irradiated module.

Non-standard settings of the front-end electronics were also studied. When the latency is increased from 130 to 250 clock cycles, the intensity at which hit losses are observed is reduced by the same factor, as expected. The reduction of the frequency of the column pair readout clock from 40 MHz to 20 MHz results in a sharp efficiency loss when the occupancy exceeds 0.14 hits per clock cycle per column pair, because some pixel hits are not transferred to the end-of-column buffers within the latency of 130 clock cycles. With the usual 40 MHz operation, hit losses due to this mechanism are not expected unless the occupancy is larger than twice this value (0.28 hits per clock cycle per column pair). The efficiency also decreases when the amplifier feedback current is changed, so that the peak of the Time-Over-Threshold distribution increases. The effect is due to the passage of a second particle through a pixel cell before the signal produced by the first event has fallen below the discriminator threshold. The efficiency loss is compatible with expectations and it is very small. For an average TOT of 15 clock cycles and the nominal B-layer occupancy, the efficiency loss due to this effect is 0.75%.

The test beam results demonstrate that at the hit rates expected for the B-Layer at the design LHC luminosity the pixel detector modules have an efficiency larger than 98%. However, it should be noted that the testbeam did simulate the high rate of hits in the modules, but did not simulate the high Level-1 rate and data transmission rate that would be expected at LHC, so it is only a partial simulation of operation at the highest luminosities.

Also, the B-layer hit detection efficiency may be reduced by a few per cent if the occupancy significantly exceeds the nominal value. This may occur for several reasons, such as track loopers at low momenta, a pp cross section at the LHC energy larger than the current estimate, or a machine luminosity exceeding the design value. Very large values of occupancy will also be reached during the heavy ion runs.

8.5 Spatial Resolution

We describe here measurements of spatial resolution performed on ATLAS Pixel modules equipped with the final production sensors and the final or nearly final readout electronics (the FE-I family of readout chips [88]). Measurements done with older prototypes have been published elsewhere [73–76].

Spatial resolution is mainly determined by the pixel cell size, the choice between analog or digital readout and the degree of charge sharing between adjacent pixels. Charge sharing is affected by intrinsic

¹³⁾These figures can be obtained rescaling the results documented in Ref. [87] to take into account the increase of the pixel long pitch from 300 μm to 400 μm and have been confirmed by simulation studies done with the updated layout.

Occupancy irradiated [hits/cp/bx]	ϵ 510689	ϵ 510852	ϵ 510910	Occupancy not irr. [hits/cp/bx]	ϵ 510929	tot [bx]	lat. [bx]	read. [MHz]	hit dupl.
0.030-0.043	0.981	0.984	0.986	0.040	0.988	15	130	40	NO
0.069-0.084	0.981	0.984	0.985	0.082	0.986	15	130	40	NO
0.100-0.124	0.980	0.982	0.983	0.124	0.983	15	130	40	YES
0.199-0.202	0.978	0.982	0.985	0.239	0.984	15	130	40	NO
0.269-0.282	0.964	0.967	0.944	0.306	0.898	15	130	40	YES

Table 14: Measurements of detection efficiency performed with a high intensity beam. The first column reports the average occupancy of the irradiated modules for the column pair on which the beam was most intense. The range corresponds to the fact that due to the different position of each module relative to the beam, the occupancy varies slightly from module to module. The second to the fourth columns report the measured detection efficiency of the three modules irradiated to 10^{15} n_{eq}cm⁻². The fifth and the sixth column report, respectively, the occupancy and the efficiency of the not irradiated module. The last columns report the front-end electronics settings, in this order: the TOT peak tuning value and the latency, the column readout frequency, and whether hit duplication was on.

sensor properties (e.g. inter-pixel capacitance and pixel capacitance to the backplane), operational parameters (such as reverse bias operating voltage and radiation damage etc.) and by parameters related to electronic readout (threshold, crosstalk, charge resolution etc.). A substantial role is also played by the incident particle track angle and by the $\vec{E} \times \vec{B}$ effect.

If there is no charge sharing, all of the charge carriers locally generated around the incident particle trajectory are collected on a single pixel (single hit clusters) and the spatial resolution is related to $\sigma = L/\sqrt{12}$, where L is the pixel pitch. If the liberated charge is collected on neighbouring pixels (two or more pixel clusters) charge interpolation becomes possible, which provides for improved resolution. The charge sharing between adjacent pixels was studied using tracks at normal incidence. The width of the charge sharing region extended from approximately ± 3 to ± 7 μm depending on the threshold, depletion depth and bias voltage (which influence diffusion).

When a particle is incident within the charge sharing region, it may generate two-pixels-clusters. This depends on sensor charge collection efficiency and the electronics threshold. Two different algorithms were used to reconstruct the spatial position of two-pixels-clusters. A *digital* algorithm which uses the center position between the two pixels and an *analog* algorithm that corrects the binary position just described using an interpolation of the charge collected by the two pixels. Since it was observed that the ratio of the charge collected on the right hand side pixel (Q_r) over the total charge collected by the two pixels $\eta = Q_r/(Q_l + Q_r)$ (where Q_r and Q_l are the charges collected by the right hand side and left hand side pixels in the cluster, respectively) had a dependence on the position of the passing particle, the following interpolation was adopted [89]:

$$x_{\text{an}} = x_{\text{dig}} + \frac{\Delta}{N_0} \int_0^\eta \frac{dN}{d\eta} d\eta \quad (1)$$

where x_{an} and x_{dig} are the spatial positions reconstructed by the analog and digital algorithms respectively. This formula assumes that N_0 particles are spread uniformly over an interval Δ that is the width of the region within which charge sharing occurs.

An equivalent procedure was adopted for multi-pixel-clusters. These occur when particles traverse the pixel sensor at an angle. For inclined particles, the charge is collected over a region approximately given by $D \times t g(\alpha)$, where D is the sensor depletion depth, and α is the angle between the particle trajectory and the normal to the sensor surface. Charged particles with large incident angles produce

signals on many pixels and the average charge per pixel decreases, despite the longer trajectory in the silicon. Since only the signal amplitudes on the edge pixels in the clusters carry information on the position of the passing particle, the digital and the analog algorithms described above were used to reconstruct the coordinate but only taking into account the first and the last pixel in the clusters [74]. Referring to (1), Δ depends on angle, cluster multiplicity and sensor design and is extracted from a fit to data for each configuration.

As the track length under a pixel is geometrically limited by $p/\sin\alpha$ (p being the pixel size), charges on a pixel exceeding $Q_{\text{cut}} = \lambda p/\sin\alpha$ (where λ is the mean number of electrons generated per unit path length) are due to energy loss fluctuations and δ electrons. The impact of these fluctuations on resolution was reduced by setting pulse heights exceeding Q_{cut} to Q_{cut} , when computing η .

In what follows, x describes the short ($50\ \mu\text{m}$) and y the long ($400\ \mu\text{m}$) pitch dimension of the pixel assembly.

8.5.1 Determination of the Telescope Extrapolation Uncertainty

Spatial resolution was determined by computing the residuals between the coordinate measured by the pixel detector and that predicted by the silicon microstrip telescope. The extrapolation uncertainty depends on many parameters, e.g. the position of the microstrip planes and of the pixel detector under study, the microstrips intrinsic resolution, the amount of material along the beam path etc. Telescope resolution was improved applying a tighter selection on track reconstruction χ^2 probability.

The resolution of the telescope can be evaluated using the residuals for both single pixel and double pixel clusters at normal incidence. An example of these distribution is reported in Figure 43. Single pixel clusters occur when incident particles cross the pixel central region of width $L=p-2*\Delta$. The distribution of their residuals can be parametrized as a uniform distribution of width L , convoluted with a Gaussian distribution that takes into account the resolution of the silicon strip telescope, threshold effects and δ -rays [84]. An alternative method to estimate telescope resolution is a Gaussian fit to the two-pixel cluster analog residuals whose width is expected to be dominated by the telescope uncertainty.

The two methods give values in statistical agreement for the telescope resolution. At 0° telescope resolution values between 3 and $6\ \mu\text{m}$ were measured, depending on the different amount of material along the beam line. At higher angles slightly worse values were measured, due to the projection on the pixel detector plane (which yields a telescope resolution proportional to $1/\cos\alpha$) and the presence of more material along the beam when detectors are tilted.

The quoted values are the standard deviations evaluated by fitting the residual distributions with a Gaussian function. These are less sensitive to statistical fluctuations than the rms and give a reasonably good description of the width of the distributions even when the distributions are not Gaussian (as occurs at angles at which a limited charge sharing is present).

8.5.2 x-Spatial Resolution at Normal Incidence

At normal incidence mainly single-pixel and double-pixel-clusters occur. The resolution is determined by their relative abundance and is dominated by the single hit cluster resolution. The combined distribution of single and double pixel clusters for the FE-I2 module shown in (Figure 43, upper plots) has a standard deviation of $12.2\ \mu\text{m}$.

The relative weights of single-pixel and double-pixel-clusters are listed in Table 15, where the results for eight FE-I modules are presented.

There is not a great difference recorded between analog and digital resolutions or between not irradiated and irradiated modules. Note that the latter were still fully depleted at the operating bias voltage of $600\ \text{V}$ (see section 8.6).

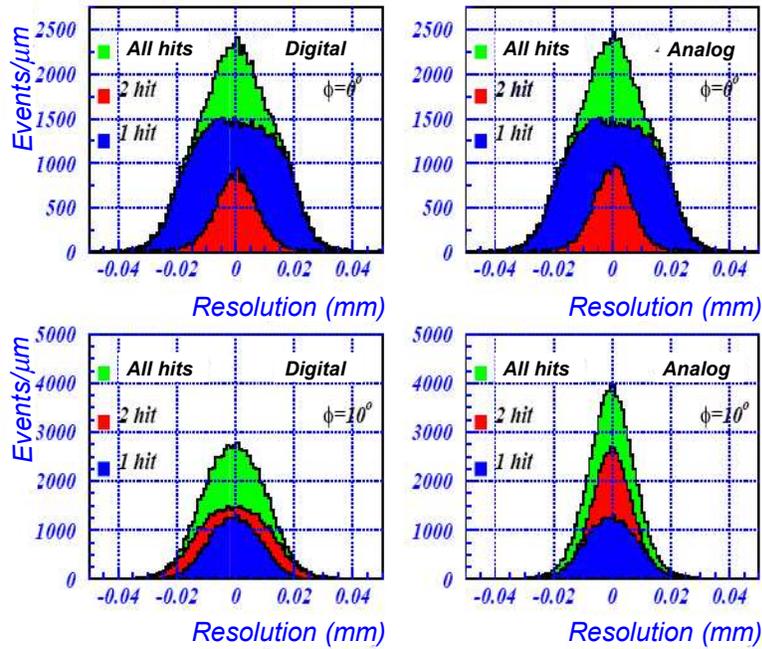


Figure 43: Left: residuals between the position measured by an unirradiated pixel detector (LBL22) using the digital algorithm and by telescope, for two different angles of incidence of the beam (0° upper plots, 10° lower plots). Different colors indicate different size of the pixel clusters. Right: residuals between the position measured by the pixel detector using the analog algorithm and by the telescope. After subtraction of telescope extrapolation uncertainty, r.m.s. are 12.2 and $12.1 \mu\text{m}$ at 0° , for digital and analog algorithms respectively, 10.1 and $7.2 \mu\text{m}$ at 10° .

Module	Irradiated	1 hits (%)	2 hits (%)	Digital resolution (μm)	Analog resolution (μm)
GE04	NO	76.3	22.2	11.8	11.7
LBL20	NO	77.0	21.5	11.6	11.4
LBL22	NO	77.0	21.1	12.2	12.1
IZMc	YES	70.1	28.8	10.6	10.3
AMS310b	YES	67.8	30.9	10.0	9.6
510929	NO	78.6	19.9	10.7	10.6
510910	YES	76.7	19.2	11.1	10.9
510689	YES	82.5	14.4	11.8	11.7

Table 15: Measurements of spatial resolution performed at normal incidence. The fraction of single and double pixel clusters is also reported. Telescope extrapolation has been subtracted.

8.5.3 x-Spatial Resolution as a function of the Angle of Incidence

Finally, the dependence of the spatial resolution on the angle α of the incident particle with respect to the normal to sensor surface was studied. The standard deviations of the all-cluster residual distributions are shown in Figure 44. The data were not corrected for the silicon microstrip telescope extrapolation uncertainty.

As the tilt angle is increased, the fraction of double pixel clusters increases, their residual distribution gets wider and the single pixel cluster distribution narrower. This is a consequence of single pixel

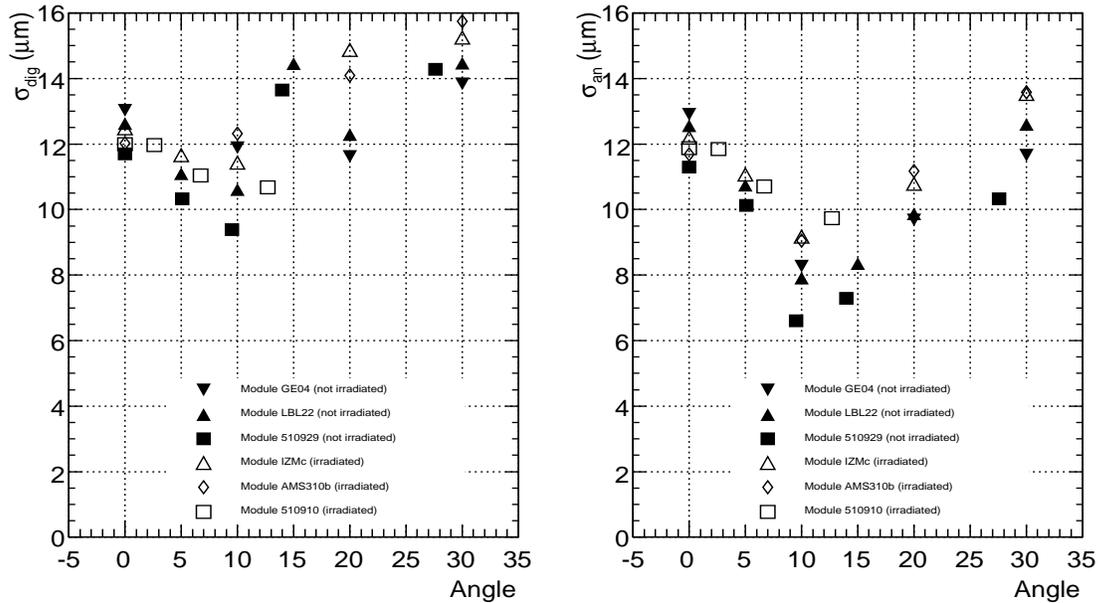


Figure 44: Measured digital (left) and analog (right) resolution as a function of the angle of incidence of the beam, without subtraction of telescope extrapolation uncertainty. The charge interpolation used by the analog algorithm allows to obtain a dramatic improvement in the spatial resolution, except that for small incidence angles when single pixel clusters are dominant.

clusters occurring in a more restricted region.

The best digital resolution is obtained when the two distributions are equally populated. At any given angle about 98 % of clusters are formed from only two multiplicities (1 and 2, 2 and 3 and so on, depending on the angle). When they are equally populated the digital resolution is of the order of $p/2/\sqrt{12} = 25 \mu\text{m}/\sqrt{12}$. When the angle is such that nearly all of the events belong to one multiplicity only, the digital resolution is of the order of $p/\sqrt{12} = 50 \mu\text{m}/\sqrt{12}$. Then the digital resolution as a function of angle (Figure 44, left plot) oscillates between these two extreme values ¹⁴⁾

The spatial resolution obtained with the analog algorithm (Figure 44, right plot and Figure 43, down right) is always better than the corresponding digital resolution once the incidence angles are larger than 0° . The charge interpolation used by the analog algorithm allows to obtain a dramatic improvement in the spatial resolution for clusters with two or more pixels. The best resolution value occurs when the proportion of single pixel clusters becomes negligible. This occurred between 10° and 15° . The best resolution for the unirradiated devices was $6.6 \mu\text{m}$ before correction for the telescope resolution. The best resolution for a device irradiated to $10^{15} \text{ nEqcm}^{-2}$ was $9.1 \mu\text{m}$ before correction for the telescope resolution. It should be noted that the spatial resolution is not significantly degraded post-irradiation, showing that there are no inhomogeneities in the sensor after irradiation. The differences in spatial resolution before and after irradiation are completely explained in terms of (a limited) reduced charge collection efficiency.

As the angle of incidence increases further, the charge collected by every pixel is reduced and energy loss fluctuations introduce inefficiencies in the first and last pixel in the cluster, thus degrading the resolution.

¹⁴⁾The silicon microstrip telescope extrapolation uncertainty was not subtracted.

8.5.4 Lorentz Angle

In the presence of an electric field and a magnetic field the charge carriers liberated by a passing particle within silicon drift along a direction at an angle Θ_L (Lorentz angle) with respect to the electric field direction, due to the $\vec{E} \times \vec{B}$ effect. This will happen in the barrel of the ATLAS Pixel detector, where the electric and magnetic field are at right angles (but not in the disks where they are parallel).

The Lorentz effect produces a systematic shift between the position of the signal induced on the electrodes and the position of the track. While this shift is in principle absorbed by the alignment correction, the knowledge of the Lorentz angle will help the understanding of the alignment corrections and their time dependence. In addition, the Lorentz effect is expected to change the angular dependence of the spatial resolution.

The Lorentz angle was measured using test beam data and a detailed report of these measurements is published elsewhere [73]. A short summary is given here.

The Lorentz angle for irradiated and unirradiated sensors was determined by measuring the minimum of the mean cluster size plotted as a function of the angle of the incident beam particles. The minimum occurs for an incident angle equal to the Lorentz angle. The results of the measurements are reported in Table 16. The measured values are compared to the predictions of a model [73, 76] which computes the Lorentz angle as a function of the magnetic field and mobility inside the sensor, the latter depending on the temperature and the electric field. A good agreement is found. Irradiated sensors have a lower Lorentz angle because a larger bias voltage is applied on a smaller depletion depth. A discussion of the Lorentz angle values expected for the Pixel Detector during operation in ATLAS can be found in [90].

Fluence ($n_{eq}cm^{-2}$)	0	$0.5 \cdot 10^{15}$	$0.5 \cdot 10^{15}$	10^{15}	10^{15}
Bias voltage (V)	150	150	600	600	600
T (K)	300	264	264	264	264
Magn. field (T)	1.48 ± 0.02	0.95 ± 0.05	0.95 ± 0.05	1.01 ± 0.05	0.74 ± 0.05
Θ_L (meas.) ($^\circ$)	$9.0 \pm 0.4 \pm 0.5$	$5.9 \pm 1.0 \pm 0.3$	$2.6 \pm 0.2 \pm 0.3$	$3.1 \pm 0.4 \pm 0.6$	$2.7 \pm 0.4 \pm 0.4$
Θ_L (th.) ($^\circ$)	9.3 ± 0.4	3.7 ± 0.5	2.7 ± 0.2	2.1 ± 0.2	1.8 ± 0.2

Table 16: Lorentz angle measurement results.

The effect of the Lorentz force on the spatial resolution is expected to be a shift of the angular dependence of the resolution on the incidence angle by an amount equal to the Lorentz angle. This has been verified with the test beam data: the spatial resolution as a function of incidence angle in presence of magnetic field was indeed similar to that obtained without field, once the angular shift was taken into account [73, 76].

8.6 Depletion Depth of Irradiated Sensors

Depletion depth of irradiated sensors is an important parameter, since its value affects detectors performance. It has therefore been studied in detail. The measurement of the depletion depth was performed according to the technique described in [73–75]. Data were taken exposing the pixels assemblies to the beam at an angle of 30° w.r.t. the normal to the pixel plane and then the average depth of charge deposition under each pixel was computed and histogrammed. The depth of charge collection region was extracted from the upper edge of this distribution. In Figure 45 the depletion depth measurements of the irradiated assemblies are shown as a function of the applied bias voltage and for three different annealing protocols ¹⁵⁾. In agreement with expectations made using the radiation damage parameters of the ROSE

¹⁵⁾The three annealing scenarios considered in the measurement and reported in the figure are: no significant annealing; the annealing which results in the minimum value of depletion voltage for a given thickness (at the end of the so called beneficial

Collaboration [91], at 600 V (foreseen operating voltage at LHC) 250 μm thick DOFZ silicon detectors are almost fully depleted after the full LHC dose after 10 years of operation and independently on their annealing history.

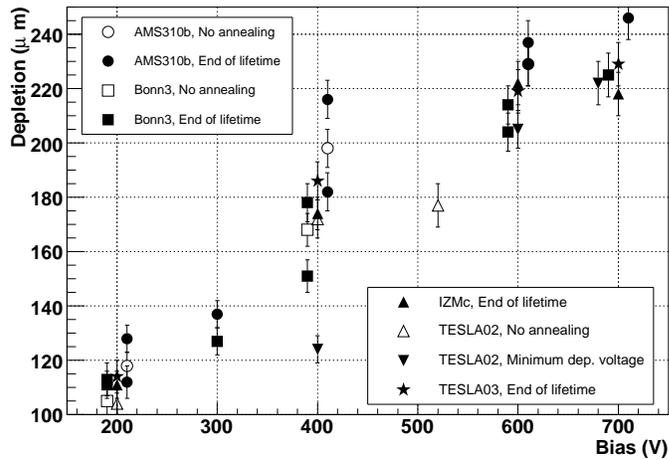


Figure 45: Measured depletion depth as a function of operating voltage for DOFZ silicon pixel detectors after irradiation of $1.1 \cdot 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$. At a bias voltage of 600 V or larger, the sensors are almost completely depleted.

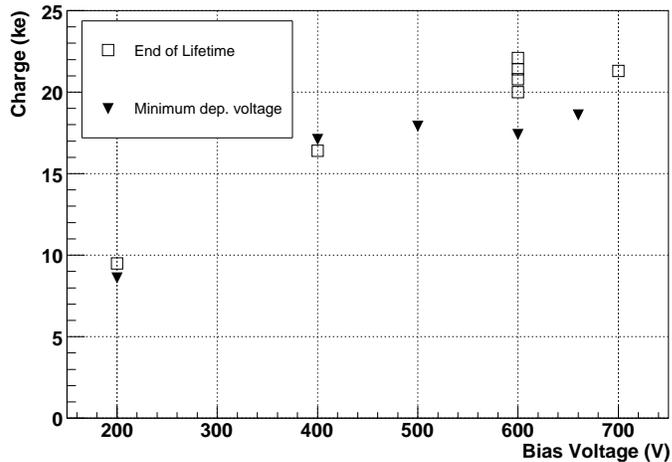


Figure 46: Average collected charge as a function of operating voltage for DOFZ silicon pixel detectors after irradiation of $1.1 \cdot 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$.

annealing); 25h of annealing at 60°C , roughly corresponding to the total annealing foreseen for the pixel detector sensors during their operating lifetime at the LHC.

8.7 Charge Collection in Irradiated Sensors

Charge collection of irradiated sensors is an important characteristics, since its value affects detectors performance, both in terms of efficiency and spatial resolution. It has therefore been measured in detail. In Figure 46 the average charge collected is shown as a function of operating voltage for irradiated assemblies. It can be noted that maximal efficiency in charge collection is reached at about 400 V by the detector annealed at the minimum value of depletion voltage V_{fd} (expected $V_{fd} = 350$ V) and its Charge Collection Efficiency does not increase at larger operating voltages, i.e. at larger electric fields. This is related to the choice of n-side readout. Since the pixel width is much smaller than the substrate thickness, most of the signal is induced by charges moving near the n-side [92], where the electric field has a maximum and the drift velocity is already saturated (i.e. independent on the electric field) at 400 V. For the detectors annealed at the end of lifetime at LHC, the plateau in charge collection is reached at 600 V (i.e. at their V_{fd}). One can notice that at the foreseen operating voltage of 600 V, the charge collected by the detectors will be well above the threshold of FE electronics. It should be noted the different asymptotic values of Charge Collection Efficiency for the two annealing protocols: at 600 V or higher operating voltage, where irradiated sensors were completely depleted, the average Charge Collection Efficiency was (87 ± 14) % (w.r.t. the one of un-irradiated sensors operating at 150 V) for sensors annealed for 25h at 60⁰ (“end of lifetime at LHC”) and (72 ± 14) % for the sensor annealed to minimum V_{fd} . The errors come from the uncertainty on charge-TOT calibration. Since detectors were completely depleted as discussed above (see depletion depth measurements), this in-efficiency is completely due to charge trapping.

8.8 Charge Trapping in Irradiated Sensors

Data taken at an angle of 30⁰ between the track and the normal to the sensor surface were also used to measure charge trapping with a new method described in [80, 93]. Because of trapping, the deeper the track segment subtended by a pixel, the lower the charge it collects. In Figure 47 the charge collected by a pixel is reported as a function of the average track segment depth for an unirradiated and two irradiated detectors. In the unirradiated detector the collected charge is constant as long as the track segment subtended by the pixel is entirely within the sensor. In the two irradiated detectors charge trapping results in a decrease of charge collection efficiency with the depth. This effect is more severe in the detector annealed to the minimum in V_{fd} than in the four detectors annealed to the end-of-lifetime scenario.

In order to be independent of the charge scale uncertainty, the charge collection profiles were normalized and only the shape of the distribution was used to investigate trapping effects. In order to extract the charge carrier lifetimes, these experimental charge collection profiles were compared to the output of a numerical simulation [92], where the interactions of charged particles with silicon were simulated using the Geant4 package [94], the drift of holes and electrons in silicon was described in detail, taking into account diffusion and trapping, and using parametrizations of literature data for the charge drift properties [95]. The signal on the pixels was computed using the Ramo theorem [96], and taking into account the electronics threshold, noise, and cross-talk.

The resulting values for the charge trapping lifetimes (assuming the same lifetime for holes and electrons) and the radiation-damage parameter $\beta = 1/\tau\Phi$ are reported in Table 17. The measurements were performed at 700 V bias voltage in order to be well above V_{fd} . The second error on trapping lifetimes in the table is the systematic error associated to the approximation of a constant electric field inside the sensor, that is correlated for different sensors. While it is difficult to precisely evaluate this correlation, there is some evidence of a dependence of the trapping probability on annealing: trapping appears to be less severe after 25h of annealing at 60⁰C than for sensors annealed to the minimum of V_{fd} . after beneficial annealing only.

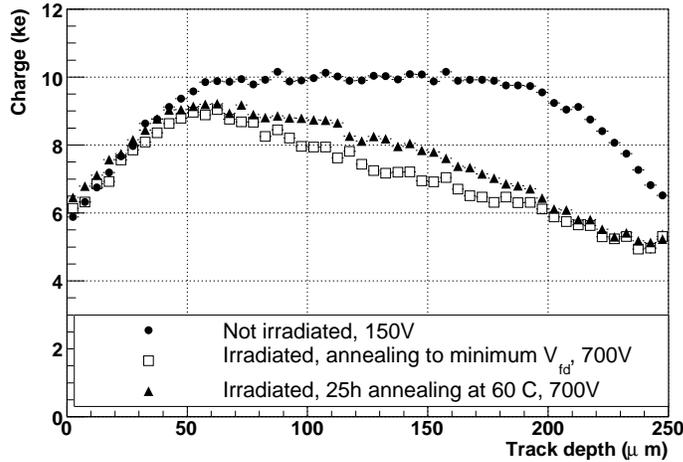


Figure 47: Pixel charge as a function of track depth for three fully depleted DOFZ silicon pixel detectors: one un-irradiated operated at 150 V and two irradiated at $1.1 \cdot 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ with two different thermal annealing levels and operated at 700 V.

Sensor	annealing	τ (ns)	β ($10^{-16} \text{ cm}^2 \text{ ns}^{-1}$)
A	25h at 60°C	$5.5 \pm 0.7 \pm 0.8$	1.7 ± 0.4
B	25h at 60°C	$3.4 \pm 0.4 \pm 0.3$	2.7 ± 0.4
I	25h at 60°C	$4.1 \pm 0.5 \pm 0.3$	2.2 ± 0.3
T3	25h at 60°C	$4.8 \pm 0.6 \pm 1.4$	1.9 ± 0.6
average	25h at 60°C	$4.1 \pm 0.3 \pm 0.6$	2.2 ± 0.4
T2	minimum V_{fd}	$2.3 \pm 0.2 \pm 0.8$	4.0 ± 1.4

Table 17: Measured values of charge trapping lifetime and radiation damage parameter β for e^- irradiated detectors at 700 V bias voltage, assuming equal lifetime for electrons and holes.

9 Combined Test Beam

During 2004, ATLAS detector modules from the Pixel Detector, SCT and TRT, the calorimeters and the Muon Spectrometer were placed in a Combined Test Beam at CERN forming a complete barrel slice of ATLAS detector [97]. The setup integrated ATLAS hardware and software in as close as possible fashion as they will be in the full ATLAS. The Combined Test Beam ran in 2004 and provided an opportunity to test the ATLAS software and to study the tracking performance using real data. The setup included six ATLAS pixel modules, placed inside a 1.4 T magnetic field. The pixel detector performed well in the Combined Test Beam, producing good quality data.

Using ATLAS offline software, tracks were successfully reconstructed. Residuals obtained after alignment showed agreement with simulation. The impact parameter and z_0 resolutions were comparable with what is expected in ATLAS.

The use of standard ATLAS components in the software chain was successful and the Combined Test Beam was a valuable development test bed for the online and offline software.

10 System Test

A system test with one endcap of the pixel detector has been performed as a realistic test of the detector operation. To achieve this goal, a setup containing about 10% of all detector services has been installed in the CERN SR1 facility. Production or pre-production parts were used as much as possible, to establish the realism of the test.

The system test program included the commissioning of the setup and the detector readout, measurements of the analogue performance of the detector modules and data taking with cosmic rays. The following sections give a brief overview of the most important procedures and results of the system test.

10.1 Setup

One endcap of the pixel detector has been operated in a system test setup. The endcap was connected to a prototype service quarter panel, as can be seen on the photo in Fig. 48, and cooled with a realistic evaporative C_3F_8 -cooling. All services connected to the endcap were made from production or pre-production parts to create a realistic copy of the final setup inside the ATLAS experiment.

The endcap was oriented vertically to optimise for data taking with cosmic rays. Several scintillators were used to generate the cosmics trigger. The scintillator arrangement, which is shown in Fig. 48, has been designed to maximise the number of triggers that have tracks passing the three disks of the endcap and at same time allow also for inclined tracks.

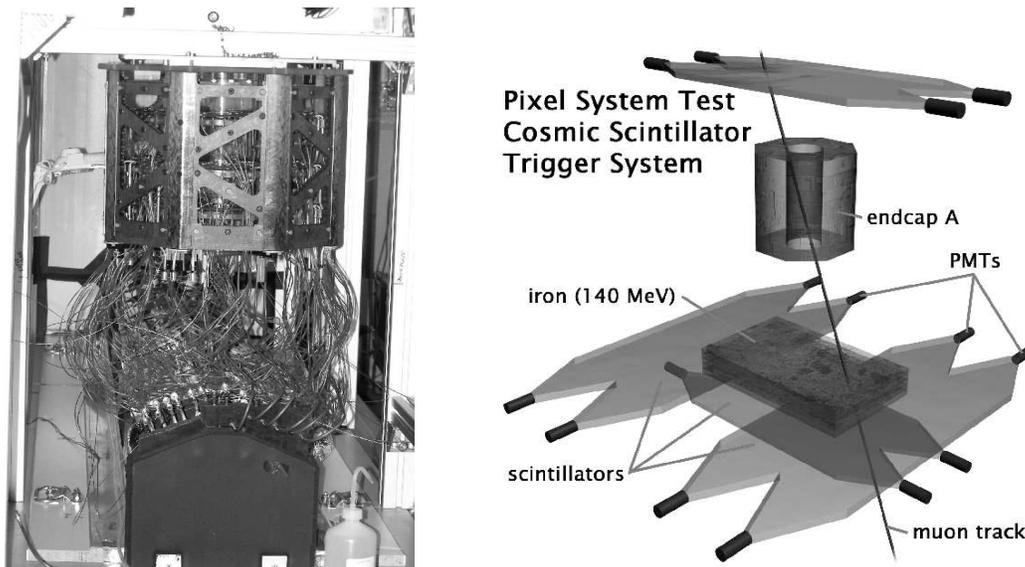


Figure 48: Photograph of the endcap in the system test setup, connected to the prototype service quarter panel, and schematic drawing of the scintillator setup for the cosmics trigger.

10.2 Commissioning of the Setup

10.2.1 Service Tests

As a first step in the commissioning of the setup, a complete test of the electrical services was performed. This was done using a dedicated test setup, which was designed to automatically test all electrical services belonging to one patch panel 0. This test protocol was a preliminary version of the services test sequence described in section 7.5.

This first application of the services test setup and procedures was essential to develop the final protocol used for services commissioning for the installed detector in ATLAS.

10.2.2 Cooling Operation

Evaporative C_3F_8 -cooling has been used for the cooling of the endcap as will be the case for the full pixel detector during operation in the ATLAS experiment. Temperature measurements at different, non-standard, supply voltages and module configurations were performed to simulate the evolving power consumption expected during the detector lifetime and assess the cooling performance under these conditions. The module temperature for power off was about -24^0 C and about -17^0 C for nominal (non-irradiated) power values and about -12^0 C extrapolated to power values after irradiation to a lifetime dose (10 years).

10.2.3 Calibration of the Optical Links

The procedures to determine the operating points of the optical links were established in part during the system test. For example, the operating point for the data links from the optoboards to the Back of Crate cards was determined from two-dimensional scans of the discriminator threshold and the phase of the data stream at the receiving end. This required that the laser power on the optoboard be set within a suitable range, which was defined by the threshold range of the receiver.

During the system test it has been found that the tuning of the data links works more reliably at higher temperatures ($\sim 20^0$ C). This is mainly due to the fact that the laser power on the optoboards is determined by a common voltage for all 6 or 7 channels and that for low temperatures the spread between the power of the different channels increases. It gets therefore more difficult to find a common operation point for all channels of the optoboard. This experience led to the introduction of special optoboard heaters into the design of the service quarter panels (section 7.4).

10.3 Analogue Performance of the Modules

Several measurements of the analogue performance of all modules were performed during the system test. Both threshold and noise values were comparable to single module measurements without any notable influence of the operation in a large scale system. Typical noise values were around 170e and the threshold dispersion after tuning was 30e - 40e.

10.4 Cosmic Ray Operation

The endcap detector has been operated with an external trigger generated from a group of scintillators arranged above and below the endcap. The rate of cosmic ray tracks crossing all three disks of the endcap in the sensitive area was about 6 Hz. The detector noise was studied [98] using several runs with different detector configuration and it was found that the noise signal was uncorrelated with the timing relative to the trigger. Pixel occupancy, i.e. the fraction of pixel hits per readout event, was used to classify “hot” pixels. Pixels with an occupancy of 10^{-5} or greater were defined as “hot” pixels. Approximately 90% of these “hot” pixels were already identified as defective during module characterization. Their total fraction is below 0.2%. After removal of “hot” pixels, the noise occupancy drops from 10^{-7} to 10^{-10} , as shown in Figure 49.

The data from cosmic ray operation were used to exercise the full chain of offline reconstruction. Digitization parameters were taken from the characterization tests performed during module production.

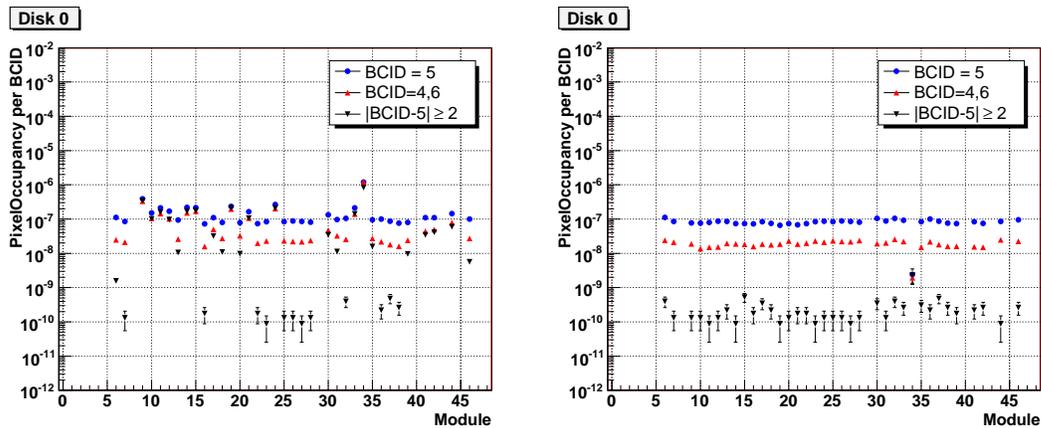


Figure 49: Occupancy per pixel in all modules of one pixel disk before (left) and after (right) masking off hot pixels for bunch crossings (BCID) within and outside the cosmic trigger (BCID=5).

The simulation produced with these parameters has been found to be in a good agreement with the data, providing an important test of the ATLAS pixel detector simulation.

The tracking studies, especially related to tracks passing through the overlap regions between adjacent modules in the same disk, have been very useful in spotting problems in the detector's geometry description and performance understanding. The characteristics of pixel clustering in the data were checked and found to agree well with the Monte Carlo simulation as shown in Figure 50.

The pixel hit efficiency was measured to be close to 100% by checking how often a pair of hits was found in the overlap region as expected. Approximately 24% of tracks crossed the overlap region, and they were used to estimate the relative alignment between the adjacent modules with the residuals of overlap hits. Figure 51 shows the resolution in the short pixel direction (LocX) before and after alignment correction. When using the nominal geometry, an initial resolution of $23 \mu\text{m}$ was obtained. After a preliminary alignment, this improves to $16 \mu\text{m}$, which is not far from the $14 \mu\text{m}$ expected from the Monte Carlo simulation. The relative alignment constants were also cross checked between the data and the survey obtained during the detector assembly (section 7.3) for the modules with enough overlap hits (≥ 50) in the data. A strong correlation between these two was found indicating that the survey is a good starting point for the final detector alignment.

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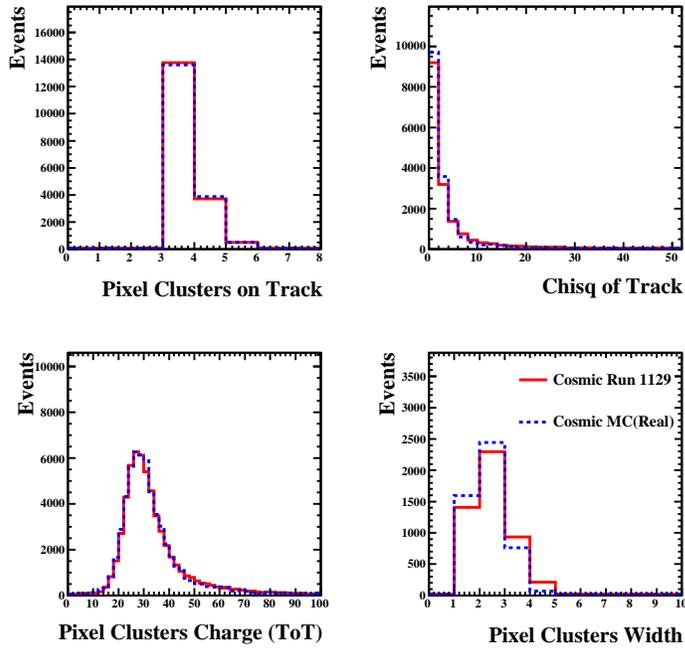


Figure 50: Comparison of the number of pixel hits and the fitted track χ^2 (top); the cluster charge of time over threshold (TOT) and the cluster width of the cosmic tracks (bottom) between data (histogram) and Monte Carlo (dashed).

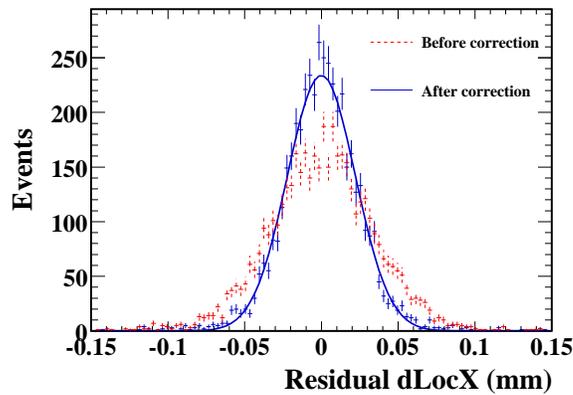


Figure 51: Distribution of overlap residual in LocX before and alignment corrections.

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